RoHS Exemption 15 Dossier For Renewal

January 16, 2015

Exemption Request Form

Date of submission: January 16, 2015

1. Name and contact details

1) Name and contact details of applicant

American Chamber of Commerce to the European Union (AmCham EU) ID number: 5265780509-97	**European Garden Machinery Industry Federation (EGMF)** ID number: 82669082072-33	**Information Technology Industry Council (ITI)** **ID number: 061601915428-87**	**LIGHTINGEUROPE** ID number: 29789243712-03
DIGITALEUROPE ID number: 64270747023-20	**European Passive Components Industry Association (EPCIA)** **ID number: 22092908193-23**	**IPC – Association Connecting Electronics Industries**	**TechAmerica Europe (TAE)** ID number: 2306836892-93
European Committee of Domestic Equipment Manufacturers (CECED) ID number: 04201463642-88	**European Semiconductor Industry Association (ESIA)** **ID Number: 22092908193-23**	Zentralverband Elektrotechnik- und Elektronikindustrie e. V. (ZVEI) ID number: 94770746469-09	**Avago Technologies**
European Coordination Committee of the Radiological, Electromedical and Healthcare IT Industry (COCIR); **ID Number – 05366537746-69**	ON Semiconductor	Freescale Semiconductor, Inc.	Pulse Electronics 12220 World Trade Drive San Diego, CA 92128 United States

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2) Name and contact details of responsible person for this application (if different from above):

Company: Intel Corporation

Name: Stephen Tisdale

Function: Manager-Industry Standards

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Chandler, AZ 85226 USA

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2. Reason for application:

Please indicate where relevant:

- ☐ Request for new exemption in:
- ☐ Request for amendment of existing exemption in:
- ☒ Request for extension of existing exemption in:
- ☐ Request for deletion of existing exemption in:
- ☐ Provision of information referring to an existing specific exemption in:
  - ☒ Annex III
  - ☐ Annex IV

No. of the exemption in RoHS Annex III or IV where applicable: #15

Existing Wording:

"Lead in solders to complete a viable electrical connection between semiconductor die and carrier within integrated circuit flip chip packages"

Proposed Wording:

"Lead in solders to complete a viable electrical connection between active component(s) and the carrier within integrated circuit flip chip packages with at least one of the following characteristics:

- Greater Than or Equal to 90nm semiconductor technology node
- Die size greater than or equal to 300mm^2 in any semiconductor technology / node (including stacked die)
- Stacked Die Packages using interposers greater than or equal to 300mm^2
- High current products (Rated at greater than or equal to 3amps) that use smaller package designs (With die sizes less than 300mm^2) incorporating the flip chip on lead-frame (FCOL) interconnect.

This wording is proposed to change from the broad scope of the existing wording to focus on the specific uses of flip chip connections which require this exemption.

Duration where applicable:

We apply for renewal of this exemption for categories 1 to 7, 10 and 11 of Annex I for an additional validity period of 5 years. For these categories, the validity of this exemption may be required beyond this timeframe. Although applications in this exemption renewal request may be relevant to categories 8 & 9, this renewal request does not address these categories. Further, categories 8 & 9 have separate maximum validity periods and time limits for application for renewals.

☐ Other: _____

3. Summary of the exemption request / revocation request

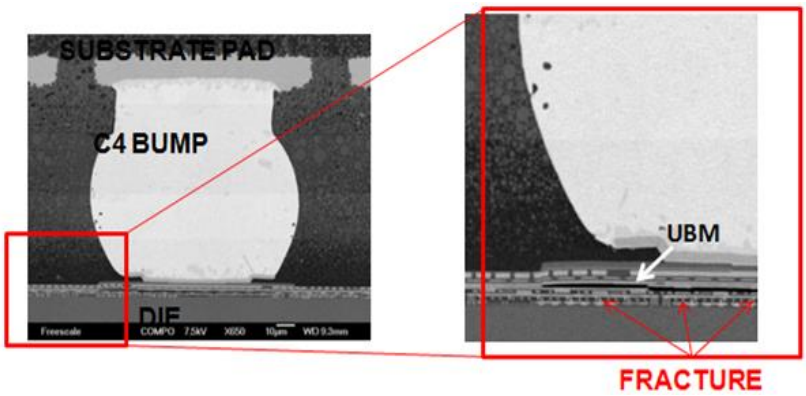
Older flip chip products, flip chip products with large die, large interposers for stacked die, and high current flip chip on lead frame package (FCOL) are not able to meet long-term reliability requirements with lead-free solder bumps on the die. Older products are defined as those having transistor gate lengths of 90nm and longer. Large die and large interposers are defined as being 300mm^2 or larger. FCOL consist of products with leads, leadless and laminate products rated at 3 amp or greater.

Silicon technology nodes with transistor gate lengths longer than 250nm used aluminum interconnect in the wafer processing backend. Later on, industry had to migrate to copper interconnect due to device performance expectations and increased circuit densities. Devices on the 250nm to 90nm technology nodes converted to a common low dielectric constant film (low-k): fluorinated tetraethyl orthosilicate (F-TEOS). F-TEOS made copper interconnect possible. At the time, F-TEOS was a breakthrough in materials engineering and from an electrical perspective it reduced capacitance in the silicon wafer backend dielectric stack. Reducing the resistance of interconnect wiring and reducing the capacitance of the interlayer dielectric (ILD) allow for higher device clock speeds. Dielectric capacitance was significantly reduced with F-TEOS when compared to the dielectrics used earlier in the semiconductor industry. The porous nature of the film is what reduces the capacitance. FTEOS offered improved electrical performance at the expense of film mechanical strength.

The low mechanical strength of F-TEOS makes it susceptible to dielectric fracturing beneath the under bump metallization (UBM) on the silicon chip (die) with lead-free wafer bumps. This does not occur with leaded C4 wafer bumps. Lead-free wafer bumps are significantly less ductile than those containing lead, and the observed failure mode mechanism is driven by coefficient of thermal expansion mismatch between the lead-free bump and the F-TEOS dielectric. Fracturing of the dielectric with Pb-free wafer bumps is commonly referred to as “ghost” or “white” bumps due to the way they appear by acoustic imaging. Not only can the failure mode reduce assembly yields, it can also adversely impact product reliability. The failure mechanism may not be caught when a unit goes through component assembly and final test. Compromised units that ship are at high risk of failing during the customer’s board level assembly process or in the field. The failure rates would be unacceptably high. This failure mode does not occur with wafer bumps that contain lead because leaded bumps are able to absorb the stress associated with the coefficient of thermal expansion mismatch between the silicon chip and the substrate to which the solder attaches. The following table compares the performance of the same product (with a die size of 98mm^2) – one with lead containing die solder to a version with lead-free die solder subjected to identical stresses. All units failed with lead-free die solder and there were not any failures with the leaded die solder.

Accelerated Stress	Process	Cycles	Temp Range (°C)	Rate of Temp Change °C/Min (Arbitrary Units)	Control Group Leaded C4 White Bumps (% Fail Units)	Pb-free C4 White Bumps (% Fail Units)
Level 0	After Die Attach	1	STD Pb-free C4 Reflow Temp	2.0 x "Y"	0%	0%
Level 1	MSL3 Reflow	3	STD Pb-free C4 Reflow Temp	3.5 x "Y"	0%	15%
Level 2	Air-to-Air Temperature Cycling (AATC)	*5	Covers Industrial and Commercial Requirements	"Y"	0%	100%

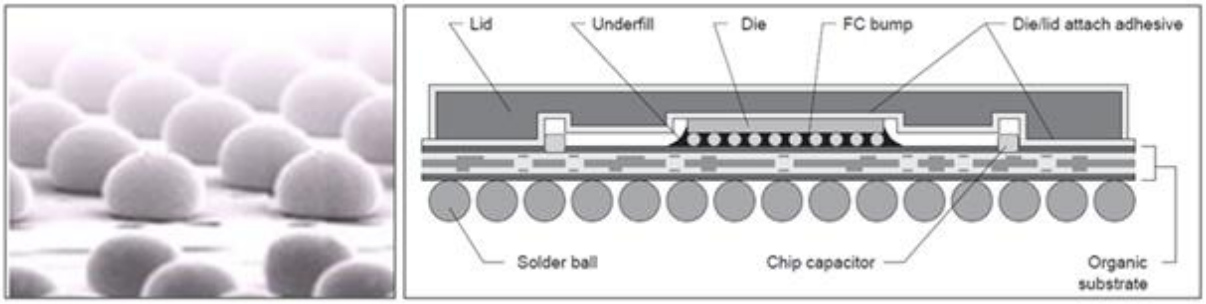
*Note: Commercial and Industrial AATC requires no failures at 400 cycles and 700 cycles, respectively.



Left Photo: Dielectric fracturing underneath a lead-free C4 wafer bump ("ghost" or "white" bump) after a chip (die) was assembled in a flip chip package. Thermal stress during the assembly process induces this failure mode. This does not occur with leaded C4 wafer bumps.

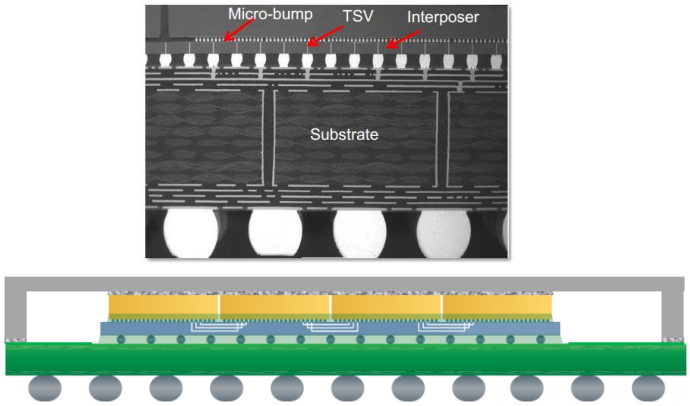
Right Photo: Magnified image of the dielectric fracture in the red box to the left. The arrows point to the delamination caused by package assembly with a lead-free wafer bump on a device with an F-TEOS backend wafer fab dielectric film stack.

Replacing the F-TEOS film with another ILD film is not an option. The entire backend wafer process integration would have to be re-engineered (e.g. dry etch; photolithography; film deposition; dielectric and copper polishes). Any change in the existing process architecture and materials would cause shifts in electrical characteristics that would force the device to have to be redesigned. There are many high reliability flip chip applications that continue to use these older silicon technologies and they typically remain in the field for over 20 years. Examples of where flip chip packages are used include: microprocessors; routing switches; servers; broadband gateways; PBX; multiplex cards; printers; gaming applications; telecom; and a variety of wireless/RF applications.



Left Photo: Flip chip solder bumps on a silicon wafer (sphere diameters are typically 80 microns or less). Refer to Section 4.2 for a comparison of flip chip packaging to wire bond packaging. The solder spheres significantly reduce the length of the interconnect (wiring) between the silicon die and the substrate, required for achieving high clock rates.

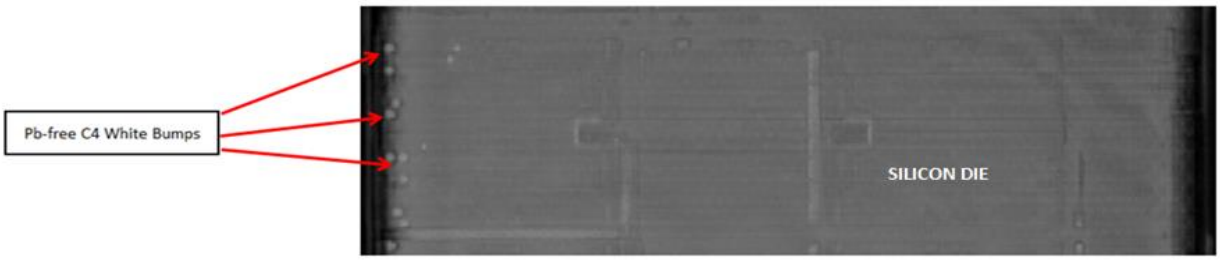
Right Drawing: Illustration of a fully assembled flip chip package. The solder balls at the bottom are used to connect the package to the end users printed circuit board.



Images Above: Cross-section of a Stacked Silicon Interconnect Technology (SSIT) or 2.5D/3D Stacked Die module with active die and passive interposer and finished package construction. Typical construction would be Cu Micro-bumps, 65nm Si technology and SnPb C4 bumps on the interposer. The finished package termination (BGA balls) would be Pb-free solder.

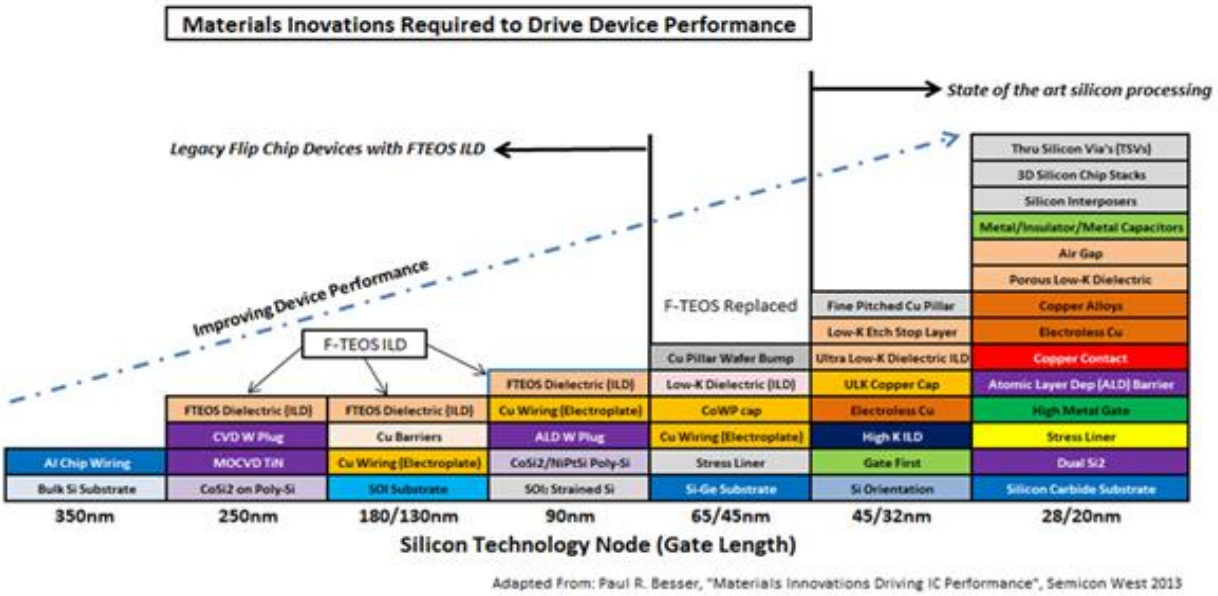
Over time, EEE consumers have expected improvements in both computing power and processing speed (i.e. higher clock rates). Transistor miniaturization and reductions in electrical resistance within semiconductor chips were required to accomplish this. Reduced electrical resistance was achieved in part by minimizing the interconnect wire length between the chip and the package. A repercussion of higher clock rates is increased power consumption by the chip which the packaged device must dissipate. Flip chip packaging was implemented to facilitate higher clock rates and heat dissipation. For instance, microprocessors that clock between 1.4GHz and 3.8GHz must dissipate between 50 and 165 Watts of power over a very small area. Achieving device performance like this is not possible with wire bonding.

The most advanced silicon technology nodes, defined as those with transistor gate lengths of 65nm and smaller completely replaced F-TEOS. These replacement technologies are designed to address the stress levels associated with lead-free die solders, except when the die size is 300mm^2 or larger. Package size increases with die size and larger packages impart significantly more strain energy onto the die and solder bump. Consequently, lead-free die solder bumps are not compatible with large die sizes even in the most advanced silicon technologies. Large die with lead-free die solder bumps near the edges and corners will deflect much more thermal and mechanical stress during fatigue cycling which can cause brittle fracture in lead-free bump alloys.



Top Image: White bumps at the edge of a die observed after Pb-free wafer bump die attach to a substrate. Non-destructive imaging with a Sonoscan D9000 acoustic microscope.

The following illustration shows innovations in materials and the materials process integration that have been required in order to drive device performance and compatibility with lead-free solder bumps on die.



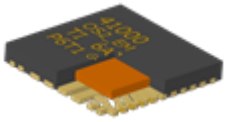
Adapted From: Paul R. Besser, "Materials Innovations Driving IC Performance", Semicon West 2013

Detailed FCOL information:

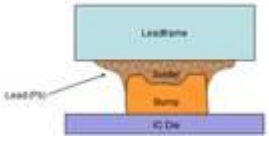
High current products (>= 3amps) that use smaller package designs (<300mm2) incorporating the flip chip on lead-frame (FCOL) interconnect.

a. The FCOL design moved from traditional wirebond material sets to flipchip package type
b. Benefits
    1. Reduced the package size and
    2. Decreased package parasitic which is a direct gain in electrical performance and
    3. Allows for higher current capabilities.
    4. The higher current capaiblities of the FCOL pacakged products expands the range of applications originally designed for cell phones and mobile devices to applications such as automotive and electronics in general.

Package Example:



Flip chip on leadframe detail:



Flip chips are commonly used in long life, high reliability applications that remain in the field for over 20 years and require continuous availability for replacement parts. Legacy flip chip devices and many large die devices are older products that have declining volume year-on-year making it difficult to justify an all-layer and material redesign. Removing these products from the market would create long supply gaps with minimal impact on the amount of lead in the EU market. Pin-for-pin compatibility replacements with devices on more recent silicon technology nodes are not available, potentially resulting in premature replacement of EEE due to lack of repair parts. The elimination of the flip chip lead solder exemption for the applications in this request would result in non-availability of mission critical components.

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4. Technical description of the exemption request / revocation request

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(A) Description of the concerned application:

1) To which EEE is the exemption request/information relevant?

Name of applications or products:

Flip chip solders within active semiconductor components that require high speed and high reliability.

i. List of relevant categories: (mark more than one where applicable)

- ☒ 1
- ☒ 2
- ☒ 3
- ☒ 4
- ☒ 5
- ☒ 6
- ☒ 7
- ☐ 8
- ☐ 9
- ☒ 10
- ☒ 11

ii. Please specify if application is in use in other categories to which the exemption request does not refer: __

Although applications in this exemption renewal request may be relevant to categories 8 & 9, this renewal request does not address these categories, therefore, we have not completed section 4(A)1.iii. Further, categories 8 & 9 have separate maximum validity periods and time limits for application for renewals.

iii. Please specify for equipment of category 8 and 9:

The requested exemption will be applied in

- ☐ monitoring and control instruments in industry
- ☐ in-vitro diagnostics
- ☐ other medical devices or other monitoring and control instruments than those in industry

2. Which of the six substances is in use in the application/product?

(Indicate more than one where applicable)

☒ Pb ☐ Cd ☐ Hg ☐ Cr-VI ☐ PBB ☐ PBDE

Function of the substance:

To complete a viable electrical connection between semiconductor die and carrier within integrated circuit flip chip packages. A viable connection must support high speed electrical

signal transfer, high heat dissipation, and/or be capable of high reliability and structural integrity during peak operating conditions.

3. Content of substance in homogeneous material (%weight):

The flip chip Pb content is a sum of two parts. The flip chip semiconductor die bumps on the silicon chip vary from the general eutectic 37% Pb to > 85% Pb by weight. The flip chip bumps also require a Pb cladding on the substrate / interposer bonding pads or solder posts on the leadframe, generally using the 37% eutectic Pb, but could range much higher to meet production processing and reliability requirements such as thermal cycling demands. During the integrated package assembly process, the Pb will interact and form a single homogeneous substance. The exact Pb % weight in the solder after assembly will vary according to the bump size, pad size, and Pb % in each material type. The final Pb content will likely be less than 85% by weight.

Example of F/C Pb Materials	% Pb Content
Silicon Flip Chip Die Bump	37% - 97%
Solder Cladding on Substrate Pad* * May not be used for ceramic	37% - 75%
Combined Flip Chip Materials after Assembly	37% - 97%

4. Amount of substance entering the EU market annually through application for which the exemption is requested:

It is currently estimated that approximately 900kg/year of lead is entering the EU due to the flip chip exemption.

The table below details the type of devices, WW shipments, and calculated lead placed on the EU market in 2014. The 2008 lead usage estimates are included for reference.

Device type	**Average Bumps per device in 2014**	WW shipments (Million Devices)		Mass of Pb(kg) into EU Markets	
		2008	**2014**	**2008**	**2014**
Server/ Mainframe	10,000	64	40	335	349
PC CPU	3,000	277	0	725	0
Games	3,500	53	0	162	0
DSP	450	23	2.5	10	1

ASIC/ Switch mix	2,000	162	22	353	38
FPGA	2,000	17	2.9	59	5
Graphics Processor	2,000	174	258	607	450
Routers	4000	36	15	63	52
TOTAL				**2315**	**896**

The lead usage calculations were based on the following assumptions:

1. An average bump pitch of 150um
2. Eutectic tin/lead solder bumps (high Pb bumps negligible volume)
3. Average bump diameter of 50um
4. 30% of WW shipments are placed in the EU.
5. Volume estimates were obtained from Techsearch International

Overall lead usage for this exemption is estimated to have reduced by 61% since 2008. It can be seen that PC processors and gaming devices have successfully eliminated leaded solder. The predominant remaining uses of leaded flip chip devices are in servers and graphics processors. Within these devices there is a trend of decreasing dependence on the use of leaded solder. Graphics processor volume from 2008 to 2014 increased from 174M to 258M units, while lead usage decreased from 607 kg to 450 kg. For server devices, the estimated lead usage decreased from 64M devices to 40M devices. Despite the decreased component count, there was a small increase in lead usage in server products due to a 67% increase in the number of L1 bumps used in these devices. The remaining devices using leaded flip chip attach are typically very large chips and/or long lived older IC technologies for which lead free designs could not be reliably produced.

The electronics industry has demonstrated a strong commitment to developing new lead free flip chip devices as new technologies with adequate reliability become available. The remaining devices manufactured in leaded flip chip attach are expected to continue declining over the next 5 years as those products are replaced with newer technology.

More Background information – Does NOT apply to FCOL

Only a limited number of Pb containing components are in production today and the volume is in a sharp decline. In the case of one company, from 2012 to 2014, the volume has dropped approximately 80% and looking forward to 2015 forecasts show it to continue to drop another approximate 5% from 2012. Exact numbers are proprietary, but if volumes were 1,000,000 components and using an average amount of lead in flip chips of 1.25mg, the total amount of lead in 2012, and projected for 2014 and 2015 are:

Year	# of Units	Total Amount of Lead
2012	1,000,000	1.25 Kg
2014	200,000	0.25Kg
2015	150,000	0.19Kg

It is fully expected these volumes continue to drop as the need to support legacy end products decreases to end of life. As can be seen from the example numbers the total amount of lead in Kg for all components is very small. These products are only being supported to meet strict customer design and safety requirements already in place before 2016. The cost to redesign and qualify a product that has very limited and greatly reduced production volume left cannot be justified nor does its environmental impact of actual total Lead justify a >$1million per instance redesign cost on existing product applications. This cost for redesign is only for the component, it does not include costs for retrofitting to customer applications which could increase this cost by 10x or more for each unique implementation.

5. Name of material/component:

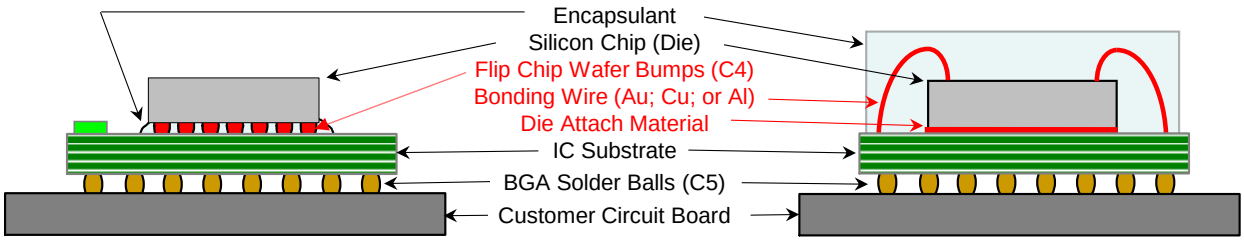
   Pb solder within integrated circuit flip chip packages.

6. Environmental Assessment:

   LCA: ☐ Yes

   ☒ No

Comparison Between Flip Chip and Wire Bond BGA Packages



DRAWINGS NOT TO SCALE

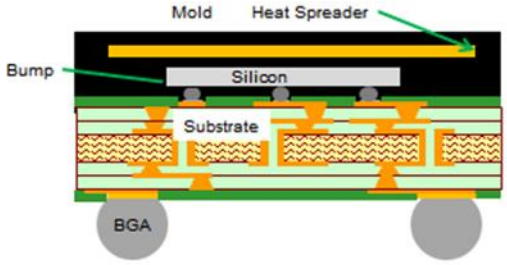
Flip Chip BGA

- Flip Chip Bumps (C4) replace bonding wire & die attach material. The shorter interconnect is required for high speed devices.
- Die larger than 300mm^2 and silicon wafer technology nodes of 90 nm and older require lead Flip Chip Bumps using ELV exemption 8g.

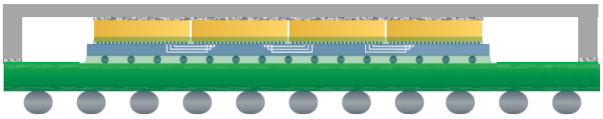
Wire Bond BGA

- Interconnect between the die and the substrate is achieved using bonding wire.
- Soft solder die attach materials containing lead are necessary for extreme thermal cycling requirements and use ELV exemption 8e.

2) In which material and/or component is the RoHS-regulated substance used, for which you request the exemption or its revocation? What is the function of this material or component?

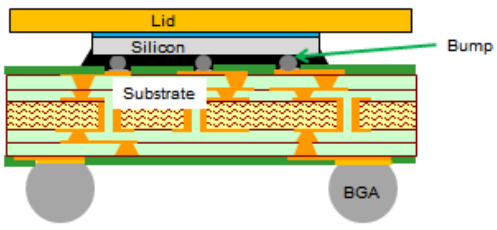


Over Molded Flip Chip

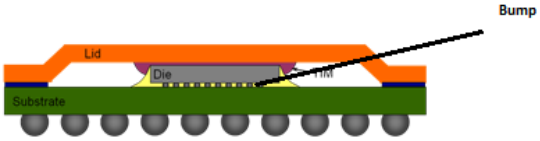


Stacked Die Packages with Large Interposers

- For silicon wafer technology nodes of 90nm and older, the overmolded lead Flip Chip Bump packaging technology was the state of the art and ramped to production.
- Flip chip bumps replace bonding wire and die attach material. The shorter interconnect is required for high speed devices



Lidded Flip Chip



- Flip chip bumps replace bonding wire and die attach material. The shorter interconnect is required for high speed devices
- Lead is required within internal solder joint to withstand higher reflow temperatures for subsequent processing

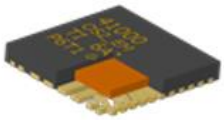
3) What are the particular characteristics and functions of the RoHS-regulated substance that require its use in this material or component?

Lower temperature melting solder minimizes internal package stresses that prevent package failures such as package material interface delamination, i.e., the glue under the chip delaminates from the package substrate. Due to its high reliability characteristics, especially in mission critical applications, this solution must remain unchanged during the life of customer's product line. No new product designs will use the overmolded product solution.

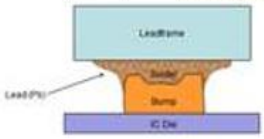
Flip Chip on Leadframe:

Package is assembled on a Pb-free profile and the Pb internal solder joint using a 60% Pb solution does not melt during the secondary 260C assembly process. By using the Pb internal solder joint, fatigue resistance to thermal cycling is much greater and resists cracking where Pb-free solutions currently fail.

Package Example:



Flip chip on leadframe detail:



5. Information on Possible preparation for reuse or recycling of waste from EEE and on provisions for appropriate treatment of waste

1) Please indicate if a closed loop system exist for EEE waste of application exists and provide information of its characteristics (method of collection to ensure closed loop, method of treatment, etc.)

No closed loop system exists for waste collection on flip chip integrated circuit packages. These components are recycled as part of the EEE into which they are incorporated. However, it should be considered the event of disposal the solder in a flip chip device inherently presents a much lower risk to the environment than many other uses of lead alloys. Flip chip devices are typically "under filled" with a chemically stable epoxy encapsulant that seals in the solder. The volume of solder used in these devices is also very small. A 500 sq mm ASIC is

estimated to contain 13.5 mg of lead. By contrast, a single car battery contains 9.7 kg of lead (equivalent to ~720,000 large ASICs).

Because of the long life time of some devices and evolving IC manufacturing processes, low volume devices may require a "lifetime buy" when the older wafer fabrication processes are retired. In these cases, the manufacturers could be entirely dependent on existing inventory that has been manufactured with design rules that required leaded solders. If these devices are unable to be used in the manufacture of new products, they would have to be disposed of and add to the electronic waste stream. In addition, many existing products on which consumers and businesses are now dependent upon would become obsolete due to unavailability of repair parts.

2) Please indicate where relevant:

☐ Article is collected and sent without dismantling for recycling

☐ Article is collected and completely refurbished for reuse

☐ Article is collected and dismantled:

- ☐ The following parts are refurbished for use as spare parts: _____
- ☐ The following parts are subsequently recycled: _____

☐ Article cannot be recycled and is therefore:

- ☐ Sent for energy return
- ☐ Landfilled

3) Please provide information concerning the amount (weight) of RoHS substance present in EEE waste accumulates per annum:

☐ In articles which are refurbished _____

☐ In articles which are recycled _____

☐ In articles which are sent for energy return _____

☐ In articles which are landfilled _____

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6. Analysis of possible alternative substances

(A) Please provide information if possible alternative applications or alternatives for use of RoHS substances in application exist. Please elaborate analysis on a life-cycle basis, including where available information about independent research, peer-review studies development activities undertaken

As is the case with most companies, for legacy packages requiring exemption 15, there is no direct Pb-free solution available. The lead (Pb) used in these packages resolved failures such as delamination, die crack and bump cracking being seen by any other solution when designed 10 or more years ago.

Pb-free efforts were focused on Package redesigns that have increased the overall component's diameter, thickness and/or ultimately mass compared to the previous Pb containing packages. Since the newer package solutions cannot maintain the form, fit and function of the legacy package technology, they are not drop in replacements.

Development costs for new flip chip devices are typically in excess of $40M. In the case of high volume consumer devices, these costs can be recovered in a relatively short period of time due to very high product volume. Because of competitive pressure, these devices will often have a life cycle of less than 18 months on the market. For lower volume devices that do not require the increased performance of the latest IC technology, the industry relies on a long product life to offset the high development and tooling cost. In the case of server and telecommunication business, many of the integrated circuits will be used for 7-10 years with only minor design changes. To maintain Form, Fit and Function minor changes cannot be ones that

1. Modify the devices height, width or length
2. Change how the connections from the device to the printed circuit board fit together.
3. Significant material changes that can affect the functionality of the device in its current package design. Going from Lead to a non-Lead solution is a major material change.

If these devices were to be continually migrated to the latest IC fabrication process, the cost of designing new ICs and qualifying them in the systems would be prohibitive for many products.

The industry has demonstrated a strong commitment to developing new lead free flip chip devices as new technologies become available. Where it has not been feasible to move old designs into new IC technologies, the remaining devices present minimal risk to the environment. The remaining devices manufactured in leaded flip chip attach are expected to decline steadily over the next 5 years as those products are replaced with newer technology.

For the reasons outlined, the industry feels that an extension of at least 5 years is required for this exemption. While the current form of the exemption is felt to be sufficient, the industry is willing to narrow the scope of the current exemption based to die size greater than 300 square millimetres or integrated circuit technologies greater than 90nm, and flip chip on leadframe. Since many FCP products are used in high reliability applications, even if the exemption is limited to large die size and older technologies, those FCP small die in new technology applications no longer under the exemption would need at least 36 months for customer qualification and supply chain transition. To eliminate this exemption for all devices prematurely would have significant socioeconomic risks associated with early retirement of critical technologies, placing EU countries at a competitive disadvantage.

(B) Please provide information and data to establish reliability of possible substitutes of application and of RoHS materials in application

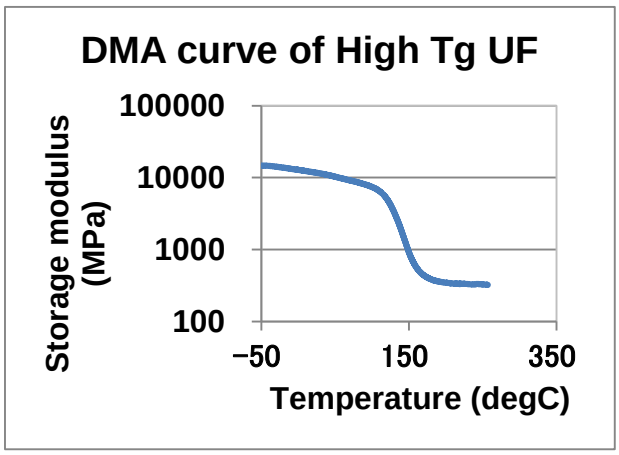
The use of lead free solder bumps in flip chip interconnects continues to be a challenge. Reliability concerns are well documented with the use of lead free solders because they are less ductile than lead solders. This causes the lead free solders to crack under stress and increases the likelihood for failures during the product life cycle. Preventing lead free solder cracks requires additional engineering to improve the thermal and mechanical fatigue life of the solder joints. The primary solution is a load-transfer from the solder to an underfill encapsulant. The residual stress from the underfill can cause other material failures which most commonly include dielectric crack,

delamination or die crack. Each component must be redesigned and tested several times to obtain the correct formulation needed to protect each layer and the solder joints.

We recognize there are industry solutions available to prevent these failures for die sizes <300 mm^2. However, solutions for large die sizes (>300 mm^2) are not available due to the increased internal stresses that require more precise engineering to prevent the same failures from occurring. When using lead free solder with large die, we have experienced similar failures as previously mentioned, but we have also experienced less common failures as discussed below.

Large die with lead free bumps requires a high glass transition temperature (Tg > 120°C) underfill (UF) to prevent solder bumps from cracking during stress tests. Figure 1 shows a typical high Tg UF with a large modulus (>10 GPa) at low temperature (<0°C). The DMA stress-strain curve shows that the storage modulus increases as the temperature decrease. The high Tg UF becomes very rigid at lower temperatures and the loss of flexibility places strain on the substrate solder mask.

Figure 1



The solder mask layer is an organic polymer used for its insulating properties to prevent solder migration. The solder mask ensures a proper connection is made between the solder bump and substrate pad.

Figure 2 and Figure 3 show that during reliability temperature cycling from -40°C to -50°C for large die the solder mask will crack due to the high stress imposed by the high Tg UF.

Figure 2: GPU (Sn/Ag bumps) ~350 mm^2

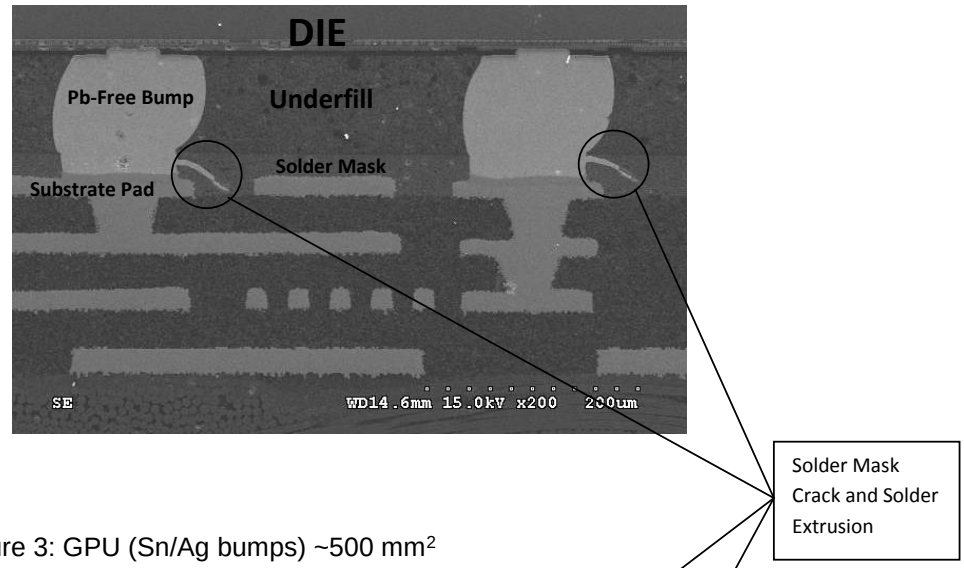
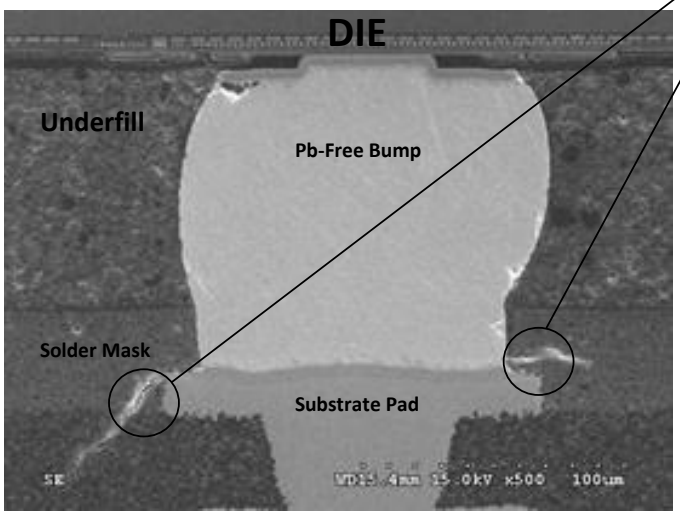


Figure 3: GPU (Sn/Ag bumps) ~500 mm^2



The crack allows for solder to extrude through the solder mask. The solder extrusion significantly decreases the package reliability due to open-short failures.

The failures shown above demonstrate that the additional strain from large die increased the failure rate for the solder mask. Ultimately, this adds another variable to the equation in developing a solution to use lead free solder or any substitute interconnection technology for large die. Our research and development is still on-going and more time is needed to find a reliable lead free solution.

References:

http://semimd.com/blog/2012/03/21/top-five-design-and-manufacturing-challenges-at-20nm/

"Citing International Business Strategies Inc. (IBS), a research firm, Cadence's Beckley said at the 32/28nm nodes, a fab runs $3 billion, process R&D is $1.2 billion,

IC design costs ranges from $50 million to $90 million, and mask costs are from $2 million to $3 million"

Challenges Associated with Large Stacked Die Flip Chip Package Assembly:

Figure 4 shows the schematic side view of a stacked silicon flip chip package. In this package, four active silicon die are connected to each other through a passive interposer with through silicon via (TSV) using micro-bumps. In this type of package, any number of active die can be assembled on the interposer and can then be connected to an organic package with C4 bumps. A capillary underfill is used to fill the gap between the micro-bumps and interposer, which helps in reducing the stress in micro-bumps. C4 bumps are created on the interposer backside, which are connected to a package substrate as shown in Figure 4. A second layer of C4 bump capillary underfill is used to fill the gap between the interposer, C4 bumps and the organic package.

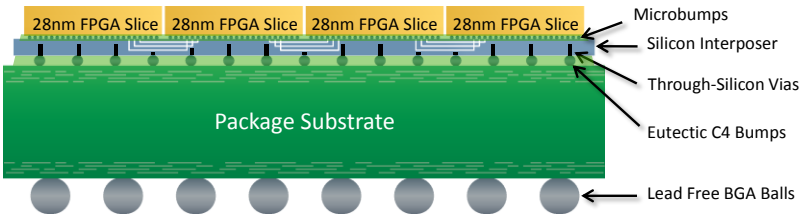


Figure: 4 Schematic Side View of Stacked Die Package or Stacked Silicon Interconnect Package without Lid

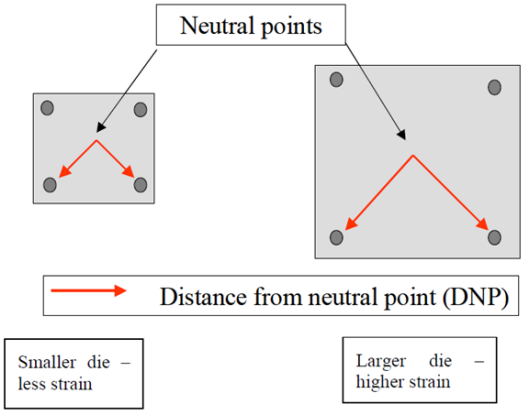


Figure 5 - Dependence of Die Size on Level of Strain (Shown by Arrows) On Corner Bumps

Size of strain on bumps is dependent on the die size and the laminate material. Most laminates have similar thermal coefficient of expansion (TCE) which is ~15ppm/°C whereas silicon has TCE of ~2.5ppm/°C. The size of the strain on bumps located at opposite corners is proportional to die size. This is referred to as the distance from the neutral point (DNP), where there is no stress at the centre of the die (DNP).

Strain is imposed by several mechanisms including device fabrication. It is particularly severe however when the component's temperature changes as a result of differential thermal expansion.

When temperature increases, the laminate expands more than the silicon and this applies a strain to the solder bump and to the materials to which these are attached.

This strain can cause damage to:

- The dielectric material that is used as insulating layers on the silicon die surface, especially if low-k dielectric materials are used.
- To the solder bonds to silicon die and to carrier circuit as a result of thermal fatigue
- To the silicon itself which may crack

As the silicon die and carrier PCB are rigidly held by the solder bumps, the effect of differential thermal expansion is to apply an outward strain on the solder bump bonds as shown by the arrows in Figure 5. The applied force is partly relieved by distortion of the silicon and package, which can "bow" outwards similarly to a "bimetallic strip" that bends when heated as a result of the different TCE values of the two metals. Therefore, as the expansion of the polymer laminate is constrained by the low TCE silicon this results in warping of these two materials. Warping causes tension on joints which can cause cracking. Underfill materials are injected between the die and carrier package to reduce strain imposed on solder bumps by spreading out the forces induced by differential thermal expansion. Underfills are designed to put solder bumps into compressive strain which prevents fatigue failure but they also increase the overall stress to the package because they have larger TCE values than the carrier material and this causes warping.

Eutectic tin/lead is a soft ductile alloy that forms strong bonds. High ductility is important as the solder deforms when a strain is imposed as a result of temperature due to the differential thermal expansion of silicon and carrier. Deformation of the eutectic tin/lead solder bumps when strain is imposed reduces the maximum level of strain on the solder joint and to the dielectric layers that form the circuitry on the silicon die. Calculations show that the maximum strain on joints imposed during thermal cycles when tin/lead solder is used is far lower than when the harder lead-free solders are used.

Lead free solders usually require underfills with higher Tg and higher modulus than eutectic solder. The main side effect of the higher Tg and modulus is that it imparts higher stress in the package and which results in higher overall package warpage. The room temperature coplanarity of a lead free stacked die package is almost two times higher than that of stacked die package with eutectic C4 bumps.

The distortion from warping causes cracking and delamination of low k dielectrics and detrimentally affects the planarity of the level 2 solder balls. If the level 2 balls do not lie in a flat plane, some (usually those in the middle) will not make contact with the PCB causing open circuits. The coplanarity of the lead free stacked die package is significantly higher than 8 mils. Research has shown that if the co-planarity of solder balls can be kept within 8 mil (0.2 mm) good bonding to the PCB is possible whereas worse co-planarity values indicate a high risk of open circuits. This value has been included in a standard published by JEDEC (Design Standard 95-1).

References:

Tin/lead and lead-free solders comparison: Jean-Paul Clech, “Acceleration Factors and Thermal Cycling Test Efficiency for Lead-Free Sn-Ag-Cu Assemblies”, SMTA International Conference, 2005.

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7. Proposed actions to develop possible substitutes

(A) Please provide information if actions have been taken to develop further possible alternatives for the application or alternatives for RoHS substances in the application.

Flip Chip:

Alternatives are readily available for new silicon wafer fabrication technologies and small die sizes. These alternatives typically use Cu studs on the die and SnAg or SAC solder on the substrate. The Cu, SnAg and SAC are more rigid than the Pb flip chip solder, introducing more stress on the products. For older technologies, large die sizes, and large interposers for flip chip stacked die this additional stress ultimately results in an unacceptably high product failure rate.

Flip Chip on Leadframe:

The industry is working on lead free solutions, but none have been able to pass the same form / fit / function requirements met by the current Pb flip chip solution.

(B) Please elaborate what stages are necessary for establishment of possible substitute and respective timeframe needed for completion of such stages.

Flip Chip:

Conversion from 90nm silicon wafer fabrication to sub-90nm fabrication requires a full product redesign, all layer mask revision, and full product qualification. It may also require modification to factory equipment and processes. Older wafer fabrication factories that are not designed for the newer equipment or clean-room standards may be shuttered.

Flip Chip on Leadframe:

Answer is the same as (A) above.

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8. Justification according to Article 5(1)(a):

(A) Links to REACH: (substance + substitute)

1) Do any of the following provisions apply to the application described under (A) and (C)?

- ☐ Authorisation
- ☐ SVHC
- ☐ Candidate list
- ☐ Proposal inclusion Annex XIV
- ☐ Annex XIV
- ☐ Restriction
- ☐ Annex XVII
- ☐ Registry of intentions
- ☒ Registration

2) Provide REACH-relevant information received through the supply chain.

Name of document:

ECHA registration dossier http://apps.echa.europa.eu/registered/data/dossiers/DISS-9c85aae9-b4e7-32ec-e044-00144f67d249/AGGR-e141b9a3-ba29-4962-80c5-be90cb034c31_DISS-9c85aae9-b4e7-32ec-e044-00144f67d249.html#section_3_5

(B) Elimination/substitution:

1) Can the substance named under 4.(A)1 be eliminated?

- ☐ Yes. Consequences? _____
- ☒ No. Justification see 6 and 7

2) Can the substance named under 4.(A)1 be substituted?

- ☐ Yes.
  - ☐ Design changes
  - ☐ Other materials
  - ☐ Other substance
- ☒ No.

  Justification see 6 and 7

3) Give details on the reliability of substitutes (technical data + information)

See reliability data under question 3.

4) Describe environmental assessment of substance from 4.(A)1 and possible substitutes with regard to
   i. Environmental impacts : _____
   ii. Health impacts : _____
   iii. Consumer safety impacts : _____
   1) Do impacts of substitution outweigh benefits thereof?

Please provide third-party verified assessment on this: _____

(C) Availability of substitutes:

1) Describe supply sources for substitutes: No substitutes exist for the revised narrow flip chip scope as described in Section 2.
2) Have you encountered problems with the availability? Describe: _____
3) Do you consider the price of the substitute to be a problem for the availability?
   a. ☐ Yes ☒ No
4) What conditions need to be fulfilled to ensure the availability? _____

(D) Socio-economic impact of substitution:

1) What kind of economic effects do you consider related to substitution?
   ☒ Increase in direct production costs
   ☒ Increase in fixed costs
   ☐ Increase in overhead
   ☐ Possible social impacts within the EU
   ☐ Possible social impacts external to the EU
   ☐ Other : _____
2) Provide sufficient evidence (third-party verified) to support your statement:

9. Other relevant information

Please provide additional relevant information to further establish the necessity of your request:

- Texas Instruments, "Flip Chip Ball Grid Array Package Reference Guide." Some illustrations and materials were obtained from this document with the approval of Texas Instruments.

10. Information that should be regarded as proprietary

Please state clearly whether any of the above information should be regarded to as proprietary information. If so, please provide verifiable justification:

none