Infinera Corporation, 169 Java Drive, Sunnyvale, CA 94089 | **T:** 408 572 5200 | **F:** 408 572 5454 | www.infinera.com

Infinera Corporation ("Infinera") provides Intelligent Transport Networks, enabling carriers, cloud operators, governments and enterprises to scale network bandwidth accelerate service innovation and simplify optical network operations. Infinera's end-to-end packet-optical portfolio is designed for long haul, subsea, datacenter interconnect and metro applications. Infinera's unique large-scale photonic integrated circuits enable innovative optical networking solutions for the most demanding networks.

The Intel, et. al., dossier for renewal of Exemption 15 primarily reflects the semiconductor industry's challenges regarding a potential expiration of this exemption and, as such, is accurate and meaningful from Infinera's perspective as a customer of that industry.

Two key issues further challenge manufacturers of long-lived, high reliability Category 3 infrastructure equipment, like Infinera:

- relatively short production lifecycles of leading edge semiconductor process technology; and
- relatively low volume of semiconductor devices we design and build on such process technology.

Semiconductor foundries (which are contract manufacturers for complex custom or semi-custom semiconductor devices) have minimum lot size requirements that can result in a single lot build producing enough devices to last a manufacturer several years. This sentence from the dossier highlights one of our key issues:

> *Since many FCP products are used in high reliability applications, even if the exemption is limited to large die size and older technologies, those FCP small die in new technology applications no longer under the exemption would need at least 36 months for customer qualification and supply chain transition.*

Regarding this sentence, we will respond to Consultation Question 2.

a. Do you agree with the scope and proposed formulation of the exemption as proposed by the applicants? Please take into account the answers to question 1 and the replacement of "semiconductor die" by "active components".

Infinera would prefer to keep the current wording of Exemption 15 for the reason stated above. The term "active components" is, as described in the Intel Response of 9 September 2015, appropriate.

Regarding question 2b.

b. Please suggest an alternative wording and explain your proposal, if you do not agree with the proposed exemption wording.

Should the wording of Exemption 15 be changed, we recommend the exemption expiration "grace period" be extended from the 12-18 months as defined in Directive 2011/65/EU, Article 5, paragraph 6, to a minimum of 36 months.

Minimum lot size orders as described above represent one issue. Another is the technology "rate of change" mismatch between Infinera's products and other semiconductor technology, which is typically driven by consumer products with much shorter product lifecycles. As a manufacturer of products that have longer product lifecycles than the semiconductor technologies used to manufacture ASICs and other integrated circuit components, Infinera's products often outlive the specific technology nodes these semiconductor (active) devices are using. This invariably results in the need for a decision between purchasing adequate "end of life" inventory to cover future sales needs (for example, for the next five years), or moving the design to a newer technology node.

Both options are expensive, but a manufacturer's decision is based on current and projected volume vs. cost. As the dossier highlights:

> *The cost to redesign and qualify a product that has very limited and greatly reduced production volume left cannot be justified nor does its environmental impact of actual total Lead justify a >$1million per instance redesign cost on existing product applications.*

Regarding question 2c.

c. Please explain why you either support the applicants' request or object to it. To support your views, please provide detailed technical argumentation / evidence in line with the criteria in RoHS Art. 5(1)(a).

Ultimately, Infinera believes there will be little actual difference in terms of direct environmental impact between the original wording and the technically justifiable proposed revision as recommended by the dossier, given the amount of lead contained in typical ASICs. However, the financial and time impact on the customers of the semiconductor industry will be significant as manufacturers with end of life inventories are suddenly unable to use them unless the Commission extends the expiration date from 12 to 18 months after the date of the decision to at least 36 months after the date of the decision, as recommended above. This will enable a smoother ramp-down of volume production and enable customers to qualify and transition to replacement technologies.

Infinera believes that 18 months is also far too short a timeframe for manufacturers to assess, justify, and fund a project to re-design/re-engineer an ASIC, receive first silicon, test and evaluate it in products, evaluate its reliability, go through customer acceptance qualifications and cut it into volume production. Again, 36 months is a far more reasonable timeframe for this.

Manufacturers like Infinera have tightly controlled budgets planned a year in advance, long term business plans and stable, well-defined business processes. Unplanned externally initiated requirements, such as the expiration of this exemption, to redesign or reengineer an important aspect of a product are typically outside the scope of a manufacturer's existing engineering budgets. These budgets are based on assessment of normal ongoing risks (changing or adding suppliers of standard multi-sourced items, addressing field issues as needed, etc.). Risk assessments of ASICs and other sole-sourced components always lead to extraordinary redesign costs or difficulties with resource allocation, and tend to result in timeline requirements as set forth here:

- Assessment of alternatives: 2 months – this requires obtaining design engineering resources, taking them off current projects, and thereby delaying, new product development (which has a time-to-market cost to the manufacturer). It can therefore take longer than 2 months based on resource availability
- Developing and justifying a budget and resource allocation: 1 month
- Engineering to tape-out (i.e., design, design verification, sending the design to the foundry): 3-6 months
- Receipt of first Silicon: 3-4 months
- Functional evaluation and testing: 1-2 months
- Reliability evaluation: 3-4 months (may be simultaneous with functional evaluation and testing)
- Customer review and acceptance: 3-5 months
- New component ramp to volume: 3-5 months
- Cut-in to revised finished good equipment, ramp to volume: 1-3 months

Any time you change a complex system of materials – and every ASIC or device moved from an existing, known reliable process to a new process is a change in a complex system of materials – a wide variety of reliability tests may be required. Often, reliability testing, including temperature cycling, high temperature life test, and so on, can be adequately accomplished, at the device level, using process test vehicles (i.e., "mock-ups" of actual product) that are designed to demonstrate worst-case characteristics. IA representative test vehicle, in this case, would be to place the largest possible die size in the target package with a high number of non-lead-based C4 bumps, particularly in corners. The customer of the device, manufacturing a system, may also need to run their own reliability tests to reflect their product's environment and the stresses induced on the device by the board to which it is attached.

The alternatives to this are:

- End of life inventories scrapped: inventory becomes useless – the particular packaging Infinera uses has little to no recoverable scrap value so will be landfilled. This is a net environmental negative, as the energy and materials used to produce the devices are ultimately wasted.
- The lead in the inventory of ASICs that end up being scrapped will go to a landfill, which is also harmful to the environment and defeats the purpose of the RoHS Directive.
- Customers in the European Union may have to wait years for replacement technologies or spend time and money qualifying alternative products because our product cannot be placed on the market.

The dossier states, accurately:

> *Flip chips are commonly used in long life, high reliability applications that remain in the field for over 20 years and require continuous availability for replacement parts. Legacy flip chip devices and many large die devices are older products that have declining volume year-on-year making it difficult to justify an all-layer and material redesign. Removing these products from the market would create long supply gaps with minimal impact on the amount of lead in the EU market. Pin-for-pin compatibility replacements with devices on more recent silicon technology nodes are not available, potentially resulting in premature replacement of EEE due to lack of repair parts. The elimination of the flip chip lead solder exemption for the applications in this request would result in non-availability of mission critical components.*

Infinera believes a minimum 36-month post-decision timeframe will enable an adequate reduction of business and reliability risks of either transitioning an ASIC or other active device from an existing technology to a replacement technology or customer transition from an existing product to a new product, which does not incorporate components using Exemption 15. Alternatively, simply retaining the current wording of Exemption 15 will have a similar effect with minimal environmental impact while allowing continued use of legacy product in high reliability, long-lived applications.