24 August, 2015

The Oeko-Institut Request Dated 16-July-2015

1st Questionnaire (Clarification Questionnaire) Exemption No. 15 (renewal request and scope restriction)

Exemption for *„Lead in solders to complete a viable electrical connection between semiconductor die and carrier within integrated circuit flip chip packages“*

Acronyms and Definitions

FCP	Flip chip package

Background

The Oeko-Institut and Fraunhofer IZM have been appointed within a framework contract[1] for the evaluation of applications for the renewal of exemptions currently listed in Annexes III of the new RoHS Directive 2011/65/EU (RoHS 2) by the European Commission.[1]

Intel et.al. has submitted a request for the renewal of the above mentioned exemption, which has been subject to a first evaluation. The information you have referred has been reviewed and as a result we have identified that there is some information missing and have formulated a few questions to clarify some aspects concerning your request before we can start the online consultation.

Please answer the below questions until 15 September, 2015 latest or otherwise let us know until when you can provide the requested information.

Questions

1) You propose the following new wording of exemption 15:
   "Lead in solders to complete a viable electrical connection between *active component(s)* and the carrier within integrated circuit flip chip packages with at least one of the following characteristics:
   - Greater than or equal to 90 nm semiconductor technology node
   - Die size greater than or equal to 300 mm^2 in any semiconductor technology/node including stacked die
   - Stacked die packages using interposers greater than or equal to 300 mm^2
   - High current products rated at greater than or equal to 3 A that use smaller package designs (with die sizes less than 300mm2) incorporating the flip chip on lead-frame (FCOL) interconnect.
   The current wording is “Lead in solders to complete a viable electrical connection between *semiconductor die* and carrier within integrated circuit flip chip packages

   Is there a specific reason why you replaced the “*semiconductor die*” of the original wording by “*active component(s)*” in your proposed new wording?

[1] Contract is implemented through Framework Contract No. ENV.C.2/FRA/2011/0020 led by Eunomia

2) You state that "The remaining devices manufactured in leaded flip chip attach are expected to continue declining over the next 5 years as those products are replaced with newer technology." You explain the problems related to a redesign of older lead-FCP. A principle alternative would be to redesign the products that still use these older lead-FCP so that they can use newer lead-free ones.
   a) What kind of products do still use lead-FCP, and what kind of FCP?

   b) Please explain the viability of this option taking into account that lead-FCP could still be used for repair and upgrade of older products that were made available on the market prior to a potential (partial) expiry of exemption 15.

3) In the table showing the worldwide shipments of products in your exemption request you use the acronyms FPGA and DSP. What do these acronyms stand for?

Please note that answers to these questions are to be published as part of the available information relevant for the stakeholder consultation to be carried out in the course of the evaluation of this request. If your answers contain confidential information, please provide a version that can be made public along with a confidential version, in which proprietary information is clearly marked. Please take into account that any recommendation on the continuation or revocation of exemption can be based on publicly available information only.

References

(Carl-Otto Gensch, Öko-Institut e. V., et al. 19 February 2009) Adaptation to scientific and technical progress under Directive 2002/95/EC: Final Report. With the assistance of Stéphanie Zangl, Rita Groß, Anna Weber, Öko-Institut e. V. and Otmar Deubzer, Fraunhofer IZM. Freiburg: . Accessed July 14, 2015. http://ec.europa.eu/environment/waste/weee/pdf/final_reportl_rohs1_en.pdf; http://ec.europa.eu/environment/waste/weee/pdf/report_2009.pdf.

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Response to Oeko-Institut 1st Questionnaire

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This response to the 9 Augusst-2015 Oeko-Institut questionnaire is submitted on behalf of myself and the participating industry associations and companies listed below.

American Chamber of Commerce to the European Union (AmCham EU) ID number: 5265780509-97	**ZVEI - German Electrical and Electronic Manufacturers´ Association** ID number: 94770746469-09	**Information Technology Industry Council (ITI)** ID number: 061601915428-87	**LIGHTINGEUROPE** ID number: 29789243712-03
DIGITALEUROPE ID number: 64270747023-20	**European Passive Components Industry Association (EPCIA)** ID number: 22092908193-23	**IPC – Association Connecting Electronics Industries**	**European Semiconductor Industry Association (ESIA)** ID Numb
European Committee of Domestic Equipment Manufacturers (CECED) ID number: 04201463642-88	**ON Semiconductor**	**Freescale Semiconductor, Inc.**	**Avago Technologies**
European Coordination Committee of the Radiological, Electromedical and Healthcare IT Industry (COCIR); ID Number – 05366537746-69	**Xilinx Inc.**	Linear Technology Corporation	

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Oeko Institut Question 1: You propose the following new wording of exemption 15:

"Lead in solders to complete a viable electrical connection between *active component(s)* and the carrier within integrated circuit flip chip packages with at least one of the following characteristics:

- Greater than or equal to 90 nm semiconductor technology node
- Die size greater than or equal to 300 mm^2 in any semiconductor technology/node including stacked die
- Stacked die packages using interposers greater than or equal to 300 mm^2
- High current products rated at greater than or equal to 3 A that use smaller package designs (with die sizes less than 300mm2) incorporating the flip chip on lead-frame (FCOL) interconnect.

The current wording is "Lead in solders to complete a viable electrical connection between *semiconductor die* and carrier within integrated circuit flip chip packages

Is there a specific reason why you replaced the "*semiconductor die*" of the original wording by "*active component(s)*" in your proposed new wording?

- The terms "semiconductor die" and "active components" are synonymous." Definitions below are from JESD88E (June 2013)
  - Active Device - A device in which at least one circuit element is an active circuit element
  - Semiconductor Die - semiconductor device (general term): A device whose essential characteristics are due, in whole or in part, to the flow of charge carriers within a semiconductor.

NOTE: For specification purposes, a semiconductor device must be considered to be either a discrete semiconductor device or an integrated circuit.

Oeko Institut Question 2: You state that "The remaining devices manufactured in leaded flip chip attach are expected to continue declining over the next 5 years as those products are replaced with newer technology." You explain the problems related to a redesign of older lead-FCP. A principle alternative would be to redesign the products that still use these older lead-FCP so that they can use newer lead-free ones.

a) What kind of products do still use lead-FCP, and what kind of FCP?

- Refer to the last sentence in paragraph 4 of Section 3 of the WG15 Exemption Extension Dossier for flip chip devices that contain lead.

  "There are many high reliability flip chip applications that continue to use these older silicon technologies and they typically remain in the field for over 20 years. Examples of where flip chip packages are used include: microprocessors; routing switches; servers; broadband gateways; PBX; multiplex cards; printers; gaming applications; telecom; and a variety of wireless/RF applications."

b) Please explain the viability of this option taking into account that lead-FCP could still be used for repair and upgrade of older products that were made available on the market prior to a potential (partial) expiry of exemption 15.

- Refer to paragraphs 1 through 4 of Section 3 of the WG15 Exemption Extension Dossier for flip chip devices that contain lead.

- "Older flip chip products, flip chip products with large die, large interposers for stacked die, and high current flip chip on lead frame package (FCOL) are not able to meet long-term reliability requirements with lead-free solder bumps on the die." (Paragraph 1 of Section 3)
- The low mechanical strength of F-TEOS (fluorinated tetraethyl orthosilicate used as a low dielectric constant film in the 250nm to 90nm technology die manufacturing nodes) makes it susceptible to dielectric fracturing beneath the under bump metallization (UBM) on the silicon chip (die) with lead-free wafer bumps. All units failed with lead-free die solder and there were not any failures with the leaded die solder. Replacing the F-TEOS film with another ILD film is not an option.

Oeko Institut Question 3: In the table showing the worldwide shipments of products in your exemption request you use the acronyms FPGA and DSP. What do these acronyms stand for?

1. FPGA – Field Programmable Gate Array : A field programmable gate array (FPGA) is an integrated circuit designed to be configured by a customer or a designer after manufacturing – hence "field-programmable"
2. DSP – Digital Signal Processor : DSP's are specialized microprocessors. They are used to measure, filter, and compress analog signals.