Review of High-Lead Solder and Lead-Glass RoHS Exemptions

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As of July 1, 2006, all applicable products in the European Union countries must comply with Waste Electrical and Electronic equipment (WEEE) and Restriction of Hazardous Substances (RoHS) legislation. The scope of the WEEE and RoHS legislations cover various household appliances, information technology and telecommunication equipment, consumer equipment, lighting equipment, electrical and electronic tools (with the exception of large-scale stationary industrial tools), toys and leisure equipment, and automatic dispensers. Medical devices, monitoring and control equipment are currently not included in the RoHS legislation, but are covered by WEEE legislation.

The RoHS legislation contains a number of exemptions from the requirement to use substitutes for hazardous (as defined in the legislations) substances. The RoHS legislation states that "exemptions from the substitution requirement should be permitted, if substitution is not possible from a scientific and technical point of view or if negative environmental or health impacts caused by substitution are likely to outweigh the human and environmental benefits of the substitution."

RoHS legislation requires that the regulations and exemptions are to be reviewed every four years. Hence, companies who currently make products that are exempted or those who are not covered by the legislation must continuously re-assess their alternatives.

This report addresses two exemptions: lead-based alloys containing eight-five percent or more lead by weight, and lead used in the glass of cathode ray tubes, electronic components, and fluorescent tubes. First, the background to the legislation and the exemptions is given and then each exemption is discussed in terms of technology. Finally, alternatives and their reliability risks are presented.

Since the RoHS legislation (including the exemptions) came into effect, technological changes have continued and our understanding of the reliability questions associated with going lead-free has improved. However, these technologies have yet to reach a stage of reliability and technical viability that warrants the removal of the relevant exemptions.

1 Background

In 1998, the European Union (EU), in response to hazardous materials being dumped into landfills throughout Europe, with resulting health risks due to environmental contamination, enacted the Waste Electrical & Electronic Equipment (WEEE) [1] directive. This in turn spawned the Restriction of Hazardous Substances (RoHS) directive. Both of these legislative measures were meant to reduce the amount of hazardous materials that ultimately end up in landfills. All applicable products in the EU market after July 1, 2006, must pass RoHS compliance [2]. All applicable products in the EU market after August 13, 2006, must meet WEEE compliance.

The scope of the WEEE and RoHS legislation extends to large and small household appliances, IT and telecommunications equipment, consumer equipment, lighting equipment, electrical and electronic tools (with the exception of large-scale stationary industrial tools), toys and leisure equipment, and automatic dispensers. Medical devices and monitoring and control equipment are currently not included in the RoHS legislation but are covered by WEEE legislation [2].

Exemptions in the legislation are granted when the substitution is technically or scientifically impracticable, or where the negative environmental, health and/or consumer safety impacts caused by substitution are likely to outweigh the environmental, health and/or consumer safety benefits of such a substitution [3]. For instance, lead-free electronics have not yet been sufficiently proven to be technically feasible in certain long-term and /or high-reliability applications. Other examples are ceramic glass frits and high-lead solders that have no cost-effective and proven alternatives.

2 High-lead solders and ceramic glass frits exemptions

The list of exemptions undergoes a mandated four-year review by the Technical Adaptation Committee (TAC) as per RoHS legislation. The Technical Adaptation Committee, comprised of representatives from EU member states, holds regular meetings to discuss issues relating to both the WEEE and RoHS directives and their implementation including consideration of new exemption requests from producers. The TAC uses various external consultants (e.g., ERA in the UK [4] [5] and Oko-Institute in Germany [10]) to help them review proposed and existing exemptions with the intention of adding, continuing, or rejecting them. An exemption under review is approved if the substitution is technically and scientifically impractical. The review also takes environment, health, and consumer safety into consideration. The exemptions relevant to this report and dates of their incorporation into the Official Journal[1] of the European Union are listed in Table 1.

Table 1: Exemptions pertaining to high-lead solders and glass frits [4] [9]

Serial Number	Exemption	Date of Incorporation[2] into Official Journal (OJ)
1	Lead in high-melting-temperature type solders (i.e., lead-based alloys containing 85% by weight or more lead)	(OJ of EU 10/21/2005)
2	Lead in solders to complete a viable electrical connection between semiconductor die and carrier within integrated circuit flip-chip packages	(OJ of EU 10/21/05)
3	Lead in solders consisting of more than two elements for the connection between the pins and the package of microprocessors with a lead content of more than 80% and less than 85% by weight	(OJ of EU 10/21/05)
4	Lead in the glass of cathode ray tubes, electronic components and fluorescent tubes	(OJ of EU 2/13/2003)

[1] The *Official Journal of the European Union* (OJ) is published every working day in all official languages of the European Union (EU) consisting of EU legislation including regulations, directives, decisions, recommendations and opinions, reports and announcements including the judgments of the European Court of Justice and the Court of First Instance, and invitations to tenders.

[2] The "date of incorporation" is the date when the exemption was last reviewed, clarified, or changed.

3 Lead-based alloys containing eighty-five percent by weight, or more, lead

Exemptions 1 and 2 listed in Table 1 were initially and predominantly intended for internal connections within flip-chip packages. Today's flip-chip packages use both high-lead as well as eutectic tin-lead solders for the semiconductor die-to- carrier (substrate) electrical attachment, and lead-free (generally SAC solders) for the external connections of the package to a printed circuit board.

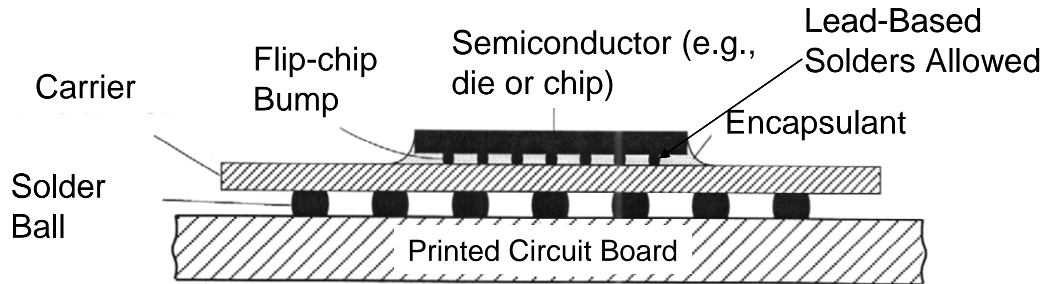

Figure 1: Schematic of a flip-chip package mounted to a printed circuit board

3.1 Reasons for exemption

Semiconductor die (chip) substrates may be ceramic or organic; but organic substrates are most common. Semiconductor die (chip) -to-carrier (substrate) connections may be achieved by various means, but the two major methods are wirebonding and flip-chip (often called controlled collapse chip connection or C4). Flip-chip offers the smallest overall size, highest I/O capacity (density), highest electrical performance and reasonable cost.

Generally, high lead content/ high melting temperature ((>85%wt), >300°C) solders are used on the chip-side bumps and lower lead content/ lower melting temperature (eutectic; 37%wt lead; 183°C) solder is used on the substrate side. The low-melting point solder component is melted, fusing it to the unmelted high-melt solder and forming an electrical joint. This allows for attachment processing at temperatures that organic carriers can sustain, in both their construction materials and their fabricated form. This is the reasoning behind the exemption for "lead in solders to complete a viable electrical connection between semiconductor die and carrier within integrated circuit Flip Chip packages" and "lead in high melting temperature solders (i.e., lead-based alloys containing 85% by weight or more lead) that are commonly used in such components" [6].

One technical hurdle for lead-free solder bumps is the under-bump metallurgy (UBM). The UBM that is conventionally used with lead-based solders may not be suitable for lead-free solders due to the difference in wettability of lead-free solders. Nickel with seven percent (by weight) vanadium, which is non-magnetic and therefore more easily deposited by magnetron sputtering, has been used successfully as a UBM with eutectic SnPb solder. However, there are serious issues with nickel-vanadium as a UBM for eutectic SAC solder due to the much higher solubility of copper in SAC. Nickel films, sputter deposited without the use of ion bombardment during deposition, are considered a potential but still immature candidate to replace nickel-vanadium as a UBM layer for use with lead-free solders [10].

There is also a process compatibility issue associated with this exemption. Conventional solder bumping processes for flip-chip include screening, evaporation, and electro-plating. Of these three, electroplating had been the method of choice in the industry to obtain fine pitch in interconnections and high current density applications cost, reliability, and yield benefits. But this process turned out to be difficult and costly to control for lead-free solders.

Several reliability studies have shown that the lead-free (SAC) alloys show comparable reliability to binary tin-lead alloys under temperature cycling [11]. Evaluation of SAC alloy solder joints under various shocks, vibrations, and high current densities, are still being conducted and reported but more time is necessary to come to a conclusion on their long-term reliability impacts.

Solders consisting of more than two elements for the connection between the pins (for pin grid array packages) and the package of microprocessors with a lead content of more than eighty percent and less than eighty-five percent by weight are also exempted until 2010. This exception was in response to an exemption request from AMD because of low manufacturing yield with lead-free solders, especially when compared to competitors' products. The claim made by AMD included several specific property requirements from this solder including melting point higher than the solder used to attach other components and being a eutectic alloy to prevent grain growth during subsequent soldering steps. The alternative solders containing antimony fared poorly in bond strengths resulting in damaged pins. The temporary exemption targeted specifically for this high (900+) pin count package provides time for the manufacturers to find alternative design, material, or process solutions [4].

3.2 Alternatives to lead and concerns with their effects on reliability

In this section, we consider available alternatives to flip-chip technology and lead-based solders in flip-chip to ensure RoHS compliance in the absence of an exemption. For each case, alternatives are introduced, followed by discussion of the associated issues. Direct chip attachment (to printed wiring board), wirebonding, use of lead free solders, new C4NP bumping process and anisotropic conductive adhesives are discussed in this section.

Direct chip attachment (DCA) also known as chip-on-board (COB) is an assembly technology in which the semiconductor die (chip) is directly mounted on and electrically interconnected to the traditional printed wiring board, instead of using semiconductor packaging technology. Since this process eliminates the internal level of solder attachment within a package – adoption of this method provides one way to eliminate the exemption. The die (chip) can be connected to the printed wiring board by several means including wirebonding, flip-chip bump soldering or conductive adhesives. This method is expensive for high volume printed wiring board assemblies, requires handling and placement of bare die by a PCB assembly company and the costs associated with yield (due to difficulty of rework) can be high.

Wirebonding is a die attachment technology that uses fine bonding wires to provide electrical connection between the die and the external leads of the package, often to a carrier. This method of attachment avoids the necessity of internal soldering. Generally, chips for wirebonding have bond pads at the periphery of the chip whereas flip-chips have I/O connections over the whole area. Consequently, compared with flip-chip interconnections, it allows much fewer I/O connections than flip-chips. Flip-chips were introduced to increase I/O capability, to reduce package sizes, and to improve the electrical performance of packages. Reverting to wirebonds to meet RoHS compliance would be a backward technical step in terms of density and speed (performance).

Another technology to attach flip-chip devices without solder bumps or balls and underfill uses anisotropic conductive adhesive films (ACFs). Conductive adhesives avoid the toxicity and environmental concerns of lead and chlorofluorocarbon-based flux cleaners, but also have technological advantages over tin-lead-based solder interconnects: (1) the lower curing temperature required for the adhesive reduces joint fatigue and stress cracking problems, enabling the use of heat-sensitive or non-solderable materials; (2) fewer processing steps enable an increase in production throughput; (3) the higher flexibility and the closer match in the coefficient of thermal expansion (CTE) enable a more compliant connection, while minimizing failures; and (4) the smaller filler particle size facilitates finer line resolution. Anisotropic conductive adhesives can also provide short electrical paths, good horizontal gap insulation, low joint stress, and sufficient mechanical adhesion. Moreover, no cleaning/flux is required, secondary underfill is not necessary, and placement of the anisotropic conductive adhesives is not critical [12]. ACF joints can maintain their low contact resistance within the incubation time during thermal cycling tests, but after the incubation time, the contact resistance will increase quickly. Most likely, ACF joints can survive general mechanical shocks up to three or four times in the absence of high temperature and humidity, but under autoclave test conditions, the survival time will decrease substantially [12]. Temperature-humidity conditions also cause stress corrosion of ACF joints, which degrades the conductivity of the joints. Without solution to these reliability issues, ACF will not be able to replace the high lead solders covered in this exemption.

IBM has developed a technology, C4NP [13], that claims to solve the processing yield issues associated with use of lead-free solders in solder bumping for use in either flip-chip in packages or in wafer-level chip-scale packages. The C4NP process can be used with any solder available in bulk metal form, including lead-free alloys [14]. This technology uses solder transfer techniques in which solder is fabricated by injecting it into prefabricated and reusable glass templates. This is followed by a screening process to ensure alignment and quality of the solder balls to achieve high yield in the transfer process that follows. SUSS Microtec, a partner of IBM in this development, announced reliability test results for C4NP in 2006. "The test was performed on 300mm wafers bumped with SnCu (tin copper) and SnAg (tin silver) solders using a 200 micron pitch with 1.3 million bumps per wafer test vehicle. Then those wafers were subjected to the following tests: moisture level, shock and vibration, deep thermal cycling (-55°C to +125°C), high temperature storage moisture stressing, electromigration, wettability, construction analysis, alpha emissions." The results claimed that none of the failures was attributable to the C4NP process [14]. These tests were performed on bumped wafers not on packages ICs with flip-chip die; thus, the reliability of flip-chips after this process is yet to be evaluated. Furthermore, this is a proprietary process developed by IBM and commercialized by only one company, Suss MicroTec [14].

Solders with high lead content on the chip to no-lead solder on the substrate are a variation of the current flip-chip assembly approach for organic substrates. This approach might use a tin-silver-copper (SAC) alloy on the substrate to connect to high-lead solder bumps on the chip [10]. Earlier, it was believed that the increase in reflow temperatures associated with lead-free solders might lead to reliability risks. However, improvements in materials and processing technologies have allayed such concerns [16]. Reliability tests are now being conducted to assess long term reliability.

3.3 Summary of the case for exemption

A key issue for the exemption for flip-chip applications was multiple assembly processes that require multiple reflows. The predominant problem that was of concern to bring about this exemption was with flip chip solder joints in a packaged device that must be soldered to a PCB. The initial view was that the solder in the flip chip should be a higher melting point than the solder connection to the PCB which is made later. Interestingly, some companies are using eutectic solder with lead-free PCB solder processes. What companies are finding is that the underfilll that is commonly used in the flip-chip protects the shape of the flip chip solder joints, even though they melt slightly during the PCB reflow process. If this process can be made technically viable in mass-production with lead free solders used in both levels, then this exemption will no longer be necessary. In that case, both the flip chip and PCB solder connection could be lead-free (based on these findings). However, more research in this area must be conducted, and it is not known whether a completely lead-free flip-chip will meet all the long-term reliability requirements.

Alternative technologies must mature and their reliability concerns must be addressed before they can be considered feasible solutions for a wide array of products and applications. Commercially available alternatives which are proprietary will raise costs considerably.

4 Lead in the glass of cathode ray tubes, electronic components, and fluorescent tubes

This exemption for lead in glass was provided because lead-free versions of these glasses have not yet been sufficiently proven for some applications. Glass frits have several applications, such as enamel barrier layers for stopping the migration of silver, in solar cells to form contacts between silver and silicon, and as a sealing material for hermetic packages. Table 2 shows several types of glass containing lead (lead oxide) and their major applications in electronic products.

Table 2: Example of lead composition and their application [17]

Glass Composition	Major Applications
$PbO-B_2O_3$	Sealing vacuum fluorescent displays, plasma display panels, fixing optical communication devices
$PbO-B_2O_3-ZnO$	Color TV bulbs, sealing vacuum fluorescent displays, sealing aluminum IC packages, insulation coating for ceramics and for insulation plates
$PbO-B_2O_3-SiO_2$	Paste material (sealing, overcoating)
$PbO-B_2O_3-Al2O_3$	Paste material (sealing, overcoating)
$PbO-SiO_2$	Sealing ferrite

4.1 Reasons for exemption

Cathode ray tubes (CRTs) are used as desktop computer displays and in televisions. The CRT display consists of a faceplate (glass panel), a shadow mask, a leaded glass funnel, and an electron gun [17]. CRT displays accelerate electrons toward a luminescent material (phosphor) that is deposited on the faceplate. The decelerating electrons produce radiation beyond acceptable levels for human health. To act as a shield against radiation, lead is added to the glass matrix in CRTs, as lead oxide. Lead oxide containing more than sixty-five percent lead is used as a radiation shielding due to its ability to absorb gamma rays and other forms of harmful radiation [18]. Lead can be found in the CRT glass parts (funnel, panel, and neck glass), the sealing frit, and the solder on the PCBs within the CRT.

Glass frit is used as a sealant in hermetic ceramic and metal electronic (semiconductor and hybrid) component packages. The lead oxide content in glass frit largely determines the properties of the frit. The coefficient of thermal expansion (CTE) of the frit can be controlled by adjusting the lead oxide content along with other ingredients, reducing the CTE mismatch and thereby making glass frits the best choice for high sintering-temperature operations. For example, US patent 6,333,116 B1 [19] shows how the CTE of glass frit can be adjusted between 7.4 to 8.5 ppm by changing the glass content 74 to 79 wt%. Hermetic electronic package manufacturers like National Semiconductor and TI produce parts that are sealed with glass frit. For example, National Semiconductor's ceramic dual inline package (schematic in Figure 2), ceramic quad package, TO-3, TO-3 and TO-39 metal-can packages all include glass seals [20].

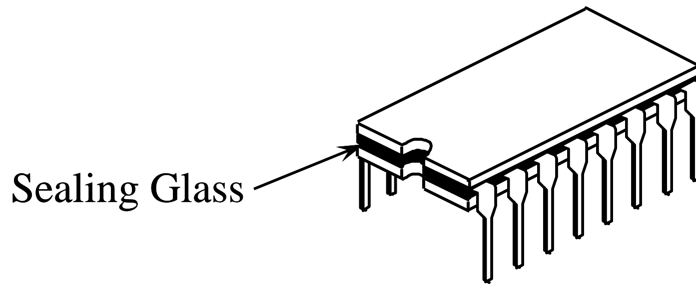

Figure 2: Hermetic ceramic dual inline package (CERDIP) assembly with frit glass seal

Lead oxide is also used in solar cells as a catalyst for contact formation. Lead-free frits in this application had been attempted since the 1970s with no success. A study in 2005 [21] developed a model to describe the formation of thick-film silver contact. The study claims that lead oxide etches through anti-reflection coating to form a mechanically stable contact. It also provides a medium for silver to grow on silicon planes, ensuring the formation of a film of silver forming a contact.

The technical adaptation committee on June 22, 2006, voted to exempt lead oxide in plasma display panels (PDP) and surface conduction electron emitter displays (SED) in structural elements, notably in the front and rear glass dielectric layers, the bus electrode, the black stripe, the address electrode, the barrier ribs, the seal frit, and the frit ring, as well as in print pastes. This exemption has now been incorporated into the Official Journal of the EU [4]. Lead oxide in seal frit used for making back light unit (BLU) lamps was exempted from RoHS in October 12, 2006, due to the absence of a technically feasible substitute [10]. In 2006, lead oxide in glass used for bonding front and rear substrates of flat fluorescent lamps used for liquid crystal displays (LCD) was also granted an exemption [4].

4.2 Alternatives to lead oxide in glass frits and reliability concerns

There is no commonly available and inexpensive substitute for lead used in CRTs. Thus, CRTs containing lead can still be manufactured, but they are subject to recycling regulations, including those of the EU and the U.S. Environmental Protection Agency (EPA) [22]. In addition, the WEEE legislation requires producers to set up separate treatment facilities to remove fluorescent coatings from CRTs.

Another area of use of glass frits is in the growing are silicon solar cells. Solar cells use lead oxides to help form a stable mechanical contact between silver and silicon. There is currently no documented alternative. However, a theoretical evaluation of the role played by the constituents of glass frit was formulated for several lead-free glass frits and evaluated to determine which of the alternatives performed as well as the lead oxide glass frits. Apparently, an alternative has been determined but the details remain proprietary information [21].

The key to finding an alternative to lead-glass frit is to understand the chemical processes involved. Several potential alternatives have been developed that modify specific properties. For example, zirconium oxide is added to reduce the boiling point [23] of glass frit. For each application, alternates need to be identified and reliability must be evaluated for that application. Reliability comparisons cannot be made based only on material properties evaluation.

For hermetic sealing of metal packages, solder can be used, but the solders are not as effective as glass frit in hermetically sealing ceramic packages.

4.3 Summary of the case for the exemption

Alternative options to the use of lead in these cases are limited and the associated risks are yet to be determined. While further research into alternatives might lead to promising results, currently the exemption is necessary. Acceptance of new exemptions for lead-based glass frits in applications such as plasma display panel (PDP), liquid crystal display (LCD) and back light unit (BLU) shows that technically feasible replacements are still in the future. To obtain hermeticity in ceramic and metal packages, the glass frit is the best accepted method at this time.

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