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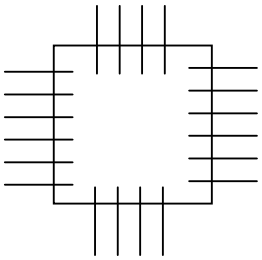
**Report: Submission to the European Commission supporting RoHS exemption No. 15**

## 1. Exemption No. 15 "Lead in solders to complete a viable electrical connection between semiconductor die and carrier within integrated circuit flip chip packages"

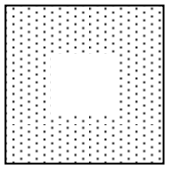
Xilinx is submitting this document to support the continuance of this exemption. The reason for the continuing need for this exemption is that to date, there are no substitutes that are technically or scientifically suitable for the larger size flip chip devices manufactured by Xilinx. It will be possible by 2010 to produce flip chip devices with silicon die that are less than 17mm along each side with lead-free solder bumps but this will not be possible for die of 17mm and larger. This submission explains why lead solders are used for flip chip bumps and why apparent substitutes are not suitable. Section 7 lists the specific data requested to support exemption 15.

## 2. Introduction

Flip chip devices have been in use for many years and pre-date the adoption of the RoHS directive in early 2003. Flip chip devices are essential where there is a need for more input and output connections required than there is space available at the edge of the silicon die only for more traditional wire bond connections.

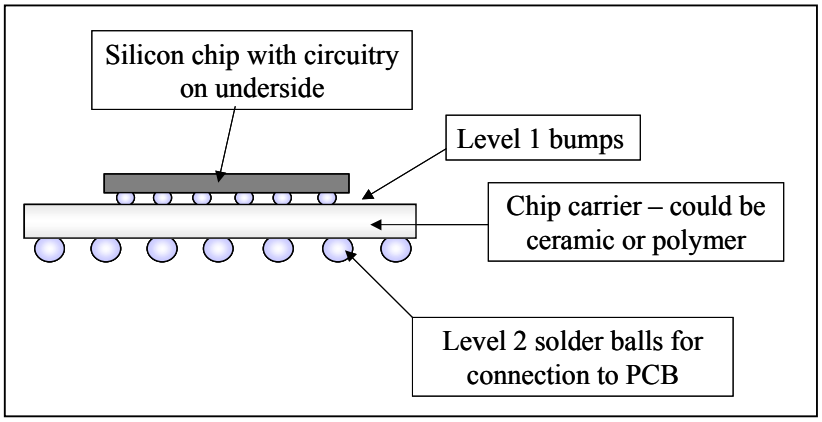


Peripheral wire bond chip



Flip chip bump bonds

A side view of a typical "flip-chip" device is shown below:




Flip-chip devices are used in many types of electrical products and may be used in equipment in all ten WEEE Directive categories as well as products that are outside the scope of RoHS such as aircraft and automotive applications.

Most devices use polymer carriers for a variety of reasons. One is that these have TCE (thermal coefficient of expansion) closer to that of the printed circuit board and this reduces the strain on the "level 2" solder balls. This however imposes a higher strain on the level 1 bumps because of the large TCE difference between that of the polymer carrier and silicon. However the strain is small and manageable with small silicon chips (<5 mm) but quite large strains are imposed with larger die and these can be sufficient to damage the bump connection, the fragile circuitry or the silicon die.

The bump connections are usually made with solder alloys that are deposited by various methods such as electroplating or solder paste printing. The deposited solder is melted on metallic pads that are part of the circuitry on the silicon chip to form arrays of bumps and these are bonded to an array of corresponding pads on small circuit boards (the carrier) that form the flip chip package. The function of the bumps is mechanical support, electrical connectivity for signals and for power and to remove heat from the circuitry. These requirements are achieved by solder as follows:

- The bumps provide mechanical support for the silicon die as well as electrical connections. Various solder alloys are used although the choice depends on a variety of variables. Often the choice is a compromise that satisfies several conflicting requirements. Alloy choice is discussed below.

- Signals – transmission of low voltage, low current and very high frequency are necessary and this requires a very low contact resistance and high electrical conductivity – only metal to metal bonds can achieve this

- Power – some modern flip chip ICs consume quite significant power levels. Power is conducted to the IC circuitry via very small bumps and so the current density through an individual bump can be very high.

- Thermal conduction – bumps made of solder efficiently conduct heat away from the chip circuitry. Some modern flip-chip BGA packages produce considerable amounts of heat and so this means of heat removal (as well as the use of heat sinks) is essential.

The need for lead in flip chip bumps was reviewed in 2004 by ERA for the European Commission[1]. ERA recommended that an exemption be granted for the reasons explained in their report and this was accepted. It is now four years later and so the need for this exemption is being re-examined by the Öko Institut for the Commission. This submission describes the results of research carried out by Xilinx and others into lead-free bump technology and explains why Xilinx believes that for certain flip chip applications, this exemption will be required for at least another four years.

## 3. Flip chip bump technology

There are many types of flip chip available on the market and an increasing proportion use lead-free solder bumps despite the existence of exemption 15. In 2004, some lead-free devices were available but as explained by ERA, these were the simpler devices which contained smaller die sizes that could use lead-free bumps because the strain is low. Also, the simpler designs do not usually use very brittle dielectric materials and so damage due to strain is not an issue. In 2004 this was not the situation with larger complex flip chip devices which could not be produced with lead-free solders because of poor reliability.

[1] ERA report from EC website http://ec.europa.eu/environment/waste/weee/pdf/era_technology_study_12_2004.pdf

Since 2004, manufacturers including Xilinx have continued to carry out research and it has been possible to broaden the range of device types that can use lead-free bumps. However research into more complex devices has also continued. Originally, lead-free bumps could not be used in larger devices because large strains imposed by thermal effects caused cracks in device and solder joints. Gradually, the resistance to cracking has been improved partly alleviated by improvements in under-fill materials that are injected around the bumps and between the die and the small carrier circuit. Some technical problems have yet to be resolved and these improvements have not yet enabled all types of flip chip to be bumped with lead-free solders. Xilinx have found from its own research that improvements in technology to date have been inadequate for largest die sizes of 17mm along each side and larger.

It has been well known since the late 1950s that the component density in electronics has increased logarithmically according to "Moore's Law". Originally this was the development of transistors which replaced thermionic valves. Component density increased significantly with the development of the integrated circuit (IC) which contains many transistors and modern ICs can contain hundreds of millions of transistors. Demands from circuit designers is continuing to result in further increases in component density on ICs and this includes flip-chip devices and this trend will continue in the future. To provide these on-going improvements, the widths of circuit track have decreased and this trend is continuing. However to continue this trend, conducting tracks need to be separated electrically with special insulators called "dielectric materials" and these must have a low dielectric constant or "low-k". Low k materials are essential to build devices which operate at higher speeds and provide superior performance that is increasingly in demand for modern electronic equipment. Low k dielectrics are softer and more easily damaged than the materials used in older technology.

Apart from improvements in under-fill materials, which is discussed in more detail below, research into alternative bump technology has continued. The main alternative approaches use copper columns being pioneered by Intel, gold bumps attached thermosonically and electrically conducting adhesives. Despite extensive research these have not been widely used by the electronics industry for the reasons discussed below (section 5).

**Technical issues with flip chip bump technology**

Flip chip technology is very complex and reliability is affected by many different variables. Some of the more important are described here.

Choice of bump solder alloy

A variety of solders are used for flip chip bumps. The most common are eutectic tin/lead, high lead content solders with 90 – 97% lead and the lead-free alloys tin/silver and tin/silver/copper.

- The high lead content alloys with 90% lead to 97% lead are used on ceramic and polymer carriers. These have superior electromigration resistance to tin-based solders and so are used where it is necessary to conduct high current densities. These alloys cannot be soldered directly onto the more common polymer laminate types because their melting point is too high and the

polymer would decompose at the melting temperature. They are bonded however to polymer carriers by soldering them with small amounts of eutectic tin/lead solder. In theory these alloys are covered by the exemption for high melting point solders but when they are attached to the carrier using eutectic tin lead solder, the lead concentration is <85%.

- Eutectic tin/lead is a soft ductile alloy that forms strong bonds. High ductility is important as the solder deforms when a strain is imposed as a result of temperature due to the differential thermal expansion of silicon and carrier. Deformation of the eutectic tin/lead solder bumps when strain is imposed reduces the maximum level of strain on the solder joint and to the dielectric layers that form the circuitry on the silicon die. Calculations show that the maximum strain on joints imposed during thermal cycles when tin/lead solder is used is far lower than when the harder lea-free solders are used[2].

- Lead-free solders are used in a growing number of flip-chip devices but these alloys have physical properties that limit their use. The most commonly used are tin/silver and tin/silver/copper both of which are considerably harder and less ductile than eutectic tin/lead or the high melting point lead alloys. Strain from differential thermal expansion of chip and carrier is therefore not reduced by solder deformation and stresses on the solder joint and dielectric materials are considerably higher than when tin/lead solder is used. A larger strain is imposed when devices are assembled also because these solders melt at a temperature of over 30°C hotter than tin/lead and this larger temperature above ambient causes more strain as a result of the difference in TCE of silicon, under-fill and carrier materials.

- The strain energy release rate (ERR) has been measured in flip-chip ICs with micro-cracks in dielectric materials. The strain energy release rate is "*the rate at which energy is absorbed by growth of the crack"* and is equivalent to the crack driving force. The ERR has been measured by the University of Texas[3] for tin/lead and lead-free solders. This showed that the strain ERR can be more than four times larger with lead-free alloys than with tin/lead solder, even with fairly small die sizes. The driving energy for cracks in dielectric layers is therefore very significantly greater with lead-free bumps than with tin/lead bumps.

Effect of Strain

Size of strain on bumps is dependent on the die size and the laminate material. Most laminates have similar thermal coefficient of expansion (TCE) which is ~15ppm/°C whereas silicon has TCE of ~2.5ppm/°C. The size of the strain on bumps located at opposite corners is proportional to die size. This is referred to as the distance from the neutral point (DNP), where there is no stress at the centre of the die (DNP) and this point.

[2] Tin/lead and lead-free solders comparison: Jean-Paul Clech, "Acceleration Factors and Thermal Cycling Test Efficiency for Lead-Free Sn-Ag-Cu Assemblies", SMTA International Conference, 2005.
[3] http://www.ae.utexas.edu/~ruihuang/Ho_Seminar2006.pdf - see also reference 5

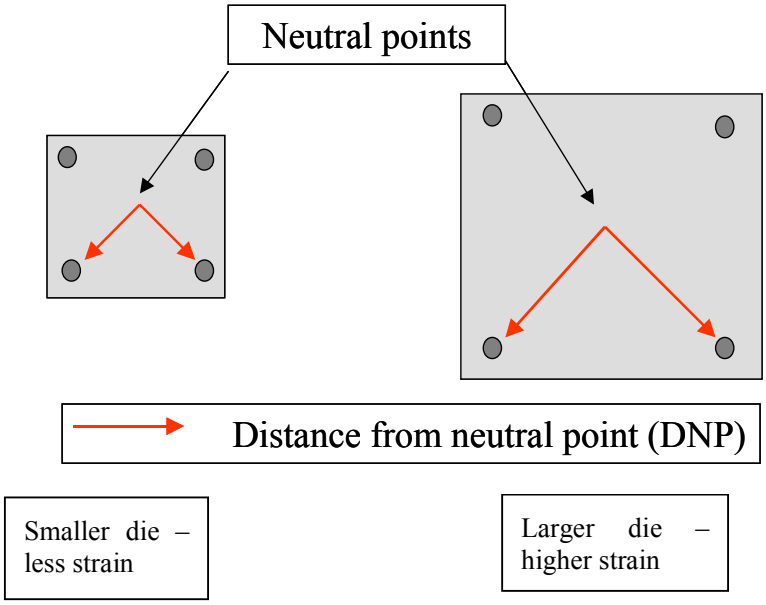



*Figure 1. Dependence of die size on level of strain (shown by arrows) on corner bumps*

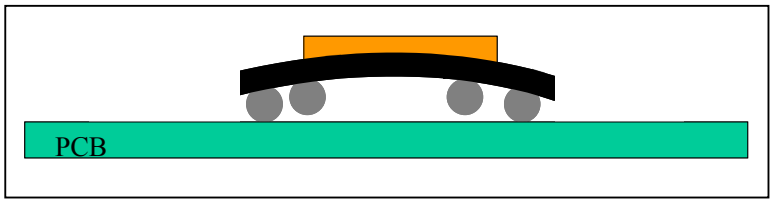
For example, a relatively small flip chip of 5 mm x 5mm square may be suitable for lead-free solder bumps as it will impose a strain that is only one quarter the size of the strain imposed on the corner bumps of a 20 x 20 mm silicon die.

Strain is imposed by several mechanisms including device fabrication. It is particularly severe however when the component's temperature changes as a result of differential thermal expansion. When temperature increases, the laminate expands more than the silicon and this applies a strain to the solder bump and to the materials to which these are attached. This strain can cause damage to:

- The dielectric material that is used as insulating layers on the silicon die surface, especially if low-k dielectric materials are used.
- To the solder bonds to silicon die and to carrier circuit as a result of thermal fatigue
- To the silicon itself which may crack

As the silicon die and carrier PCB are rigidly held by the solder bumps, the effect of differential thermal expansion is to apply an outward strain on the solder bump bonds as shown by the arrows in Figure 1. The applied force is partly relieved by distortion of the silicon and PCB which can "bow" outwards similarly to a "bimetallic strip" which bends when heated as a result of the different TCE values of the two metals. Therefore, as the expansion of the polymer laminate is constrained by the low TCE silicon this results in warping of these two materials. Warping causes tension on joints which can cause cracking. Under-fill materials (discussed below) are injected between the die and carrier to reduce strain

imposed on solder bumps by spreading out the forces induced by differential thermal expansion. Under-fills are designed to put solder bumps into compressive strain which prevents fatigue failure but they also increase the overall stress to the package because they have larger TCE values than the carrier material and this causes warping. The distortion from warping causes cracking and delamination of low k dielectrics and detrimentally affects the planarity of the level 2 solder balls. If the level 2 balls do not lie in a flat plane, some (usually those in the middle) will not make contact with the PCB causing open circuits. Research has shown that if the co-planarity of solder balls can be kept within 8 mil (0.2 mm) good bonding to the PCB is possible whereas worse co-planarity values indicate a high risk of open-circuits. This value has been included in a standard published by JEDEC (Design Standard 95-1, section 14, June 2000).




Exaggerated view of effect of warping on solder ball co-planarity – inner balls fail to bond to PCB

Low k dielectric issues

In most cases with modern large high-density flip-chip devices, the low-k dielectric material is the most susceptible to cracking. Modern high performance flip-chip devices that utilise very high density electronics have several layers of conductors separated by low-k dielectrics. Conductors in consecutive layers are connected with metallised vias that pass through the dielectric layers. High speed and performance are possible only by the use of dielectrics which have a very low dielectric constant "low-k". A variety of dielectric materials have been developed to achieve the required performance. Originally silica was used which has a dielectric constant of 4.2. Today, dielectrics with values of less than 2.7 are required and so materials such as silica are not suitable[4]. One of the materials that have very low-k is air but of course this alone is impossible to use but the properties of air can be utilised by the use of ceramic foam. Silica foam that contains a high proportion of minute air bubbles has a dielectric constant typically of 2.1. This would provide the necessary structure and a low-k but unfortunately is a fairly brittle material that cannot withstand a high strain. A variety of other dielectric materials has been developed based on organo-silicates which are weak glassy materials but having low dielectric constants. Even lower k materials have been developed which are porous organo-silicates such as methylsilsesquioxide (MSQ)

The weak and brittle nature of dielectrics may be damaged when subjected to a high strain. Many of these materials have TCE values that are larger than silicon and so are subjected to strain as a result of the difference in TCE of silicon and the dielectric and this can cause cracking and delamination. Even

[4] http://www.ae.utexas.edu/~ruihuang/Ho_Seminar2006.pdf

higher strains are imposed as a result of strain imposed by inflexible bumps due to the large TCE difference between silicon and polymer carrier. It is impossible to produce large die size flip-chip because of damage caused by this strain and it has been necessary for many years to reduce the size of the imposed strain by the use of under-fill materials.

Under-fill materials

Stresses to solder bumps and low k dielectrics are imposed by the dielectric deposition process, by the bump application process and as a result of subsequent temperature changes. Stresses are imposed on solder bump bonds because of the differential expansion of die and carrier and this can be reduced by the use of under-fill materials. However, under-fill cure involves heat that induces strain, particularly to the dielectrics which can delaminate as a result[5]. Under-fill materials are specially designed adhesives, usually epoxy resins, that bond to the laminate, the underside of the flip chip and to the bumps. Typical TCE values of the materials are:

- Silicon die ~2.5 ppm/ºC
- Carrier laminates ~15 ppm/ºC
- Lead-free under-fill ~30 ppm/ºC

Under-fills are designed to support the solder bumps by spreading out the forces from differential thermal expansion but this is achieved at the expense of stresses being applied to the package itself causing it to warp and the stress imposed on the low k dielectric causes cracking and delamination. Under-fills designed for softer tin-lead do not need to provide as much support as those designed for harder lead-free alloys. Therefore lead-free under-fills tend to be harder and stiffer and impose more stress than those formulated for tin/lead bumps. Research has shown that under-fills formulated for tin/lead can protect solder bumps so that in severe thermal cycling tests, they can survive over 1000 cycles and the co-planarity of the level 2 balls is acceptable, even with the largest die sizes. However, the stiffer under-fill materials formulated for lead-free bumps impose much higher stresses into the packages, especially with larger die sizes. These can survive 1000 severe thermal cycles without cracks in solder bumps, but co-planarity is unacceptable.

Research has also shown that high Tg (glass transition temperature) under-fill materials give improved fatigue life to solder bumps which is particularly important with large silicon die but high Tg materials are more likely to cause die cracks[6]. There are unfortunately conflicting requirements for under-fills with large die sizes. Low-stress under-fills cause less damage to dielectrics but do not prevent bump fatigue failure from thermal cycles. More rigid under-fills that support die bumps cause high package warpage

[5] "Chip-packaging interaction and reliability impact on Cu/low k interconnects" G. Wang, X. Zhang and P. S. Ho, AIP Conference vol 817, p 73, 2006.
[6] "The reliability impact of highly temperature-dependent underfill material to the lead-free flip chip package" Thermal, Mechanical and Multiphysics Simulation and Experiments in Micro-Electronics and Micro-Systems, 2006. EuroSime 2006. 7th International Conference Publication Date: 24-26 April 2006

and high stress to low k dielectrics leading to cracks and delamination as well as failing the co-planarity requirements.

Under-fill materials are essential for flip-chip devices but their development always follows progress in the design of flip-chip technology and to date Xilinx have been unable to identify under-fill materials that are suitable for the use of lead-free solder bumps with flip-chip devices having die of 17 mm and larger.

## 4. Results of Xilinx research.

**Test conditions**

Xilinx are a manufacturer of flip-chip devices including several very complex devices which have unusually large silicon die. Xilinx use low k dielectrics to achieve the speed and performance characteristics demanded by its customers and it is possible to produce devices with large die and having high reliability and long life but only if tin/lead bumps are used. Xilinx are carrying out research with lead-free bumps (tin/silver is the standard alloy used by the electronics industry for flip chip bumps) but even with the latest under-fill materials, reliability has been poor which results in premature failure and the planarity of level 2 balls is inadequate.

**Test 1.**

Xilinx have carried out tests using four different under-fill materials with 20mm die on 40 mm packages and SnAg bumps to determine if the JEDEC co-planarity specification of 8.0 mil (0.2mm ) maximum could be achieved. As heat causes differential thermal expansion, under-fill A was cured at a lower than standard temperature to reduce strain and so limit warping. As shown below this improved co-planarity but still exceeded the maximum 8 mil limit.

Test 1 results:

The co-planarity of the 20mm devices were measured after cure with four under-fill materials, results were as follows:

| Under-fill | Number of devices constructed | Maximum co-planarity (mil) |
|---|---|---|
| A | 19 | 9.09 |
| A cured at a lower temperature | 19 | 8.12 |
| B | 24 | 8.28 |
| C | 30 | 9.25 |
| D | 30 | 9.35 |

None of the underfill materials achieved the JEDEC specification of 8 mil maximum. Also, the co-planarity was found to vary considerable with minimum values being as low as 5.57 and as high as 7.91 which means that there is considerable variation in dimensions and a high risk of open-circuits.

**Test 2:**

Xilinx have also evaluated lead-free bumps with die dimensions 23mm x 23 mm and 45nm silicon technology; this is the highest component density currently available commercially. These devices use standard flip-chip construction and Xilinx have evaluated all commercially available under-fill materials with SnAg bumps. Assembled devices have been tested using industry standard test procedures involving a severe thermal cycle from –55°C to +125°C. Thermal cycling involves repeated temperature changes and because of the difference in TCE of silicon, underfill and substrate, this imposes large stresses on the die and the dielectric layers. In these tests, stiffer lead-free under-fill materials were chosen to enable the devices to survive 1000 severe thermal cycles. 1000 thermal cycles from –55°C to +125°C is regarded as the minimum that should be achieved for flip-chip devices although devices made with tin/lead solder can usually achieve 2000 cycles.

Test 2 results

In tests carried out with the 23 mm die described above, the first failures (bond failures) occurred after about 1200 cycles which just passed the minimum industry requirement (1000 minimum). However these devices failed the JEDEC co-planarity specification with an average maximum of ~ 9 mil. Although they passed the thermal cycling test criteria, the performance was inferior to what would be achievable with tin/lead bumps indicating that product lives would be shortened. Examination of the premature failures showed that this was due to cracking of the under-fill material as a result of large substrate warpage and subsequent corner delamination. Delamination of dielectric occurs at corner bumps where the strain is the highest as shown in Figure 2.

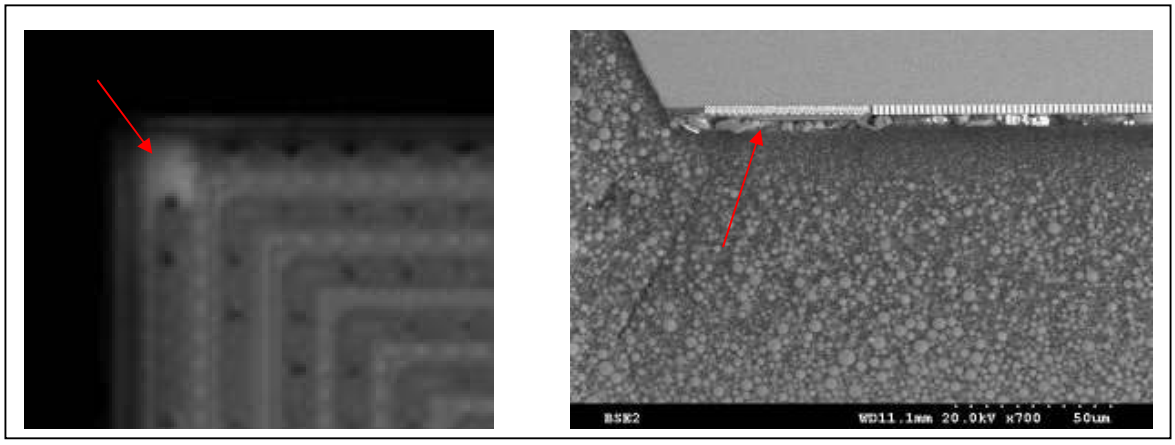


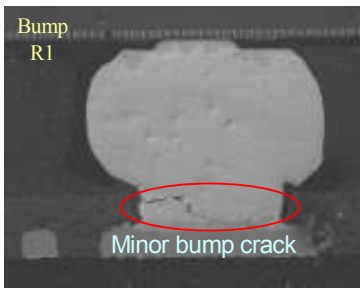

*Figure 2. Delamination of low k dielectric*

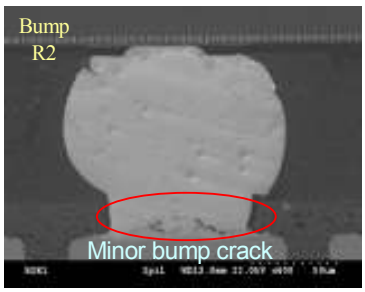
**Test 3:**

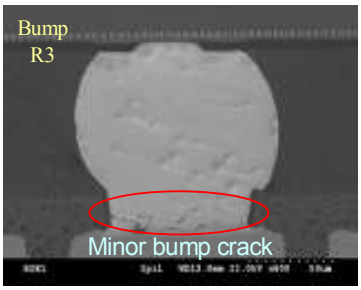
Two under-fill materials were compared in tests with 16 x 16 mm die having low k dielectric and lead-free (SnAg) solder bumps. One of the under-fills was the more flexible tin/lead type that does not cause dielectric delamination or cracking and the other was the more rigid type developed for lead-free solders. Flip chip packages were tested over 1000 severe thermal cycles.

Test 3 results:

| Under-fill type | Thermal cycling test result | |
|---|---|---|
| | **Effect on solder bumps** | **Effect on package** |
| Flexible | Cracks after < 500 cycles (see image below) | No damage to dielectric and warpage < 8 mil |
| More rigid | No cracks after >1000 cycles | Unacceptable warpage, plus delamination and cracking of low k dielectric |



## 5. Suitability of alternative bonding technology

There are several lead-free solders other than tin/silver and tin/silver/copper that are not used for flip-chip bumps and the reasons are explained below. One manufacturer has recently introduced copper post technology and there are also research publications describing gold bumps and conducting adhesives and these are described here.

**Tin/silver and tin/silver/copper** – both are much harder and more brittle than tin/lead solder alloy and so do not deform under strain which is transferred to the bump bond connection to the device.

**Tin/zinc** – This has recently been developed as a lead-free solder. Originally this could not be used as no suitable fluxes have been developed. This alloy is used in some lap top computers but very few other products. Although it is a eutectic alloy and so is less hard than tin/silver, it is very susceptible to corrosion and so field life is expected to be short. As a result of this severe limitation, it has not been considered as a suitable material for flip chip bumps.

**Tin/silver/bismuth** – this alloy is used by a few manufacturers for soldering devices with terminal pins but as it contains silver, it is hard and brittle and so suffers from the same issues as tin/silver.

**Gold** – traditional periphery connection ICs, as shown in section 2 use gold connections that are bonded using heat and ultrasonic energy (thermosonic). Research using simpler die has been carried in which gold bumps are applied and good results are reported. However, this has not been widely commercialised and this indicates that very high yields, which are essential, may not be achieved. Also, gold is relatively hard and so would suffer from the same limitations as tin/silver. The other reason why gold bumps cannot be used on flip-chip with low k dielectrics is that the thermosonic energy would damage the fragile low k materials.

**Conducting adhesive** – These materials are increasingly used in electrical equipment, for example to make electrical connections to liquid crystal displays but unfortunately they have limitations that prevent their use in the more advanced flip-chip devices. They are unsuitable for high performance and high speed flip-chip devices because the contact resistance is too large. Another limitation of conducting adhesive is the stability of electrical conductivity of the contact pads on both the silicon die and on the carrier PCB. These may be of copper, aluminium or a thin porous gold coating over nickel. High electrical conductivity is permanently maintained by a solder bond but where the bond is physical contact, the contact resistance increases as copper, aluminium and nickel all oxidise to give electrically insulating oxides. This occurs even with under-fill materials as these allow oxygen diffusion.

**Copper post with lead-free solder** – Intel recently announced that their flip-chip devices will use this new lead-free technology[7]. This development has resulted from many years research to develop new devices that use copper columns with tin/silver/copper solder instead of traditional solder bumps to bond to carrier laminates. Intel design and manufacture their own flip-chip devices whereas Xilinx and most

[7] http://www.intel.com/pressroom/kits/45nm/leadfree/lf_backgrounder.pdf

other IC producers do not own production facilities and have to rely on commercial sub-contractors to build their products. At present, the Intel copper post technology is not commercially available and so Xilinx and other fabless IC producers could not use it. The copper post with tin/silver/copper connections are very rigid materials and so would impose high stress levels and so is unlikely to resolve the problem that protection of the bump bonds and low k dielectric layers by stiff under-fill causes the co-planarity to be unacceptable. As far as Xilinx are aware, Intel die sizes that use the new copper post connections are less than 17 mm along each side. Intel has been able to use smaller die, which can utilise lead-free technology in its products by adopting 45nm technology so that the die circuitry can be fitted onto a smaller area.

## 6. Conclusion

Research to develop lead-free flip-chip bump technology has been carried out since 2004 and Xilinx expect that it will be possible to manufacturer reliable devices having smaller die size (<17 mm along each side) by 2010. The development of reliable flip-chip devices with die size of 17 mm along each side and larger has not been possible with lead-free solder bumps. This is due to the conflicting demands to protect the fragile low k dielectric materials, prevent bump cracks and meet co-planarity requirements. Lead-free solders are considerably harder than tin/lead and so require stiffer under-fill materials to prevent fatigue cracks. However the stiffer under-fill materials induce larger stresses into the package causing worse warping and delamination of the low k dielectric layers. No other technology available today is able to provide reliable flip-chip devices having large die sizes except for tin/lead solder.

## 7. Additional information

**Amount of lead used:**

Amount of lead per application on average, each Xilinx flip-chip device will contain 0.005 grams of lead as a constituent of the solder bumps.

Lead content of solder bumps used by Xilinx – 37% lead

Xilinx estimate that the total quantity of lead in its Flip Chip devices with silicon die of 17 mm and larger that were placed on the EU market in 2007 was < 10 kg of lead

**Changes since 2004** – this is discussed in detail in the above sections of this submission. There has been a lot of research into lead-free substitutes and an increasing number of flip-chip devices having smaller die sizes are now able to use lead-free solder bumps. However, this is not yet possible for the more demanding applications with larger die. There is a constant demand for higher speeds and increased performance from flip chip ICs and this has resulted in the development of lower k dielectrics which are more brittle and more easily damaged than higher k materials. Research has shown that devices fail prematurely if lead-free solder bumps are used. New under-fill materials designed for lead-free bumps

have been developed since 2004 but these are unsuitable for devices with the largest die sizes as they cause unacceptable warping and dielectric delamination.

**Use of lead-free bumps in flip chip**

Lead-free solder bumps can be used in flip-chip devices with smaller die of less than 17 mm along each side. The reliability of these may not be identical to devices made with tin/lead solder but should be acceptable by 2010. As explained above, if lead-free bumps are used on larger die, the reliability is not acceptable as these significantly shorten the life of the product. This would result in equipment (computers, mobile phones, etc.) becoming waste much sooner than is currently experienced.

**Applications where exemption 15 will continue to be needed**

Exemption 15 will continue to be required in the foreseeable future for flip-chip devices having die that are 17mm along each side and larger. These devices are used as components in products in all ten WEEE categories.

**Roadmap**

In the future, the trend to develop faster flip-chip devices with higher performance will continue. In parallel, research will continue into the development of improved more robust low k dielectric materials, more effective under-fill materials that support lead-free die bumps with a lower risk of dielectric delamination. New low k dielectrics will be fragile materials and all lead-free bumps technologies use hard brittle materials and so it might not be possible to resolve the current reliability problems without the development of a significantly new approach. At present no such development is foreseeable. Therefore based on current technology, it will be possible for flip-chip with die sizes of less than 17 mm along each side to use lead-free solder bumps, it is anticipated from 2010 but no date can yet be predicted for a lead-free solution for larger die sizes.

**Possible expiry date**

At present it is not possible to predict an expiry date for this exemption for all types of flip chip devices for the reasons explained in the previous question “roadmap”. However, it should be possible to restrict exemption 15 after 2010 to cover only the more complex types of flip chip with die of 17mm along each side and larger.

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