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Institute for Applied Ecology

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Adaption to scientific and technical progress under Directive 2002/95/EC

Results previous evaluation
Exemption No. 7 a

"a) Lead in high melting temperature type solders (i.e. lead-based alloys containing 85 % by weight or more lead)

b) lead in solders for servers, storage and storage array systems, network infrastructure equipment for switching, signalling, transmission as well as network management for telecommunications

c) lead in electronic ceramic parts (e.g. piezoelectronic devices)"

(Excerpt from ERA report 2004)

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2.9 Lead in high melting temperature type solders (i.e. tin-lead solder alloys containing more than 85% lead) and any lower melting temperature solder required to be used with high melting temperature solder to complete a viable electrical connection" and "Lead in solders to complete a viable electrical connection internal to certain integrated circuit packages (Flip Chips) (exemption until 2010)

These two exemption requests are both principally for internal connections within flip chip packages although the first of these could have other applications. Unfortunately the first request does not specify the applications to which it is intended to apply. This creates a risk that it could be used for applications for which a lead-free alternative exists or that it may be misinterpreted for widespread use of any low melting point solders.

Electrical connections are made to most silicon ICs using very thin gold wires attached to circuitry on the silicon surface. These are attached to pads at the periphery of the silicon chip. Chips are becoming more complex, however, with a need for an increasing number of electrical connections and to have connections from locations other than the chip's periphery. Also, semiconductor chips have become larger and the packages around them smaller, so to meet these requirements, an alternative means of electrical connections was required. This has been achieved by replacing the gold bond wires with raised metal "bumps" attached to pads across the surface of the silicon. These "bumped" chips are then "flipped" over (hence the name flip chip) to make electrical connections between the chip and the "chip carrier" which is essentially a small circuit board which acts as an interface between the chip and the PCB. Some flip chip are attached directly to the PCB without a carrier, these are called direct chip attach (DCA).

It is now possible to have hundreds or thousands of connections to the silicon chip, which may be up to 25 mm along each side. The solder joints between the chip and the carrier are called "Level 1" interconnections. There is another layer of solder connections between the carrier and the printed circuit board called "Level 2" interconnections.

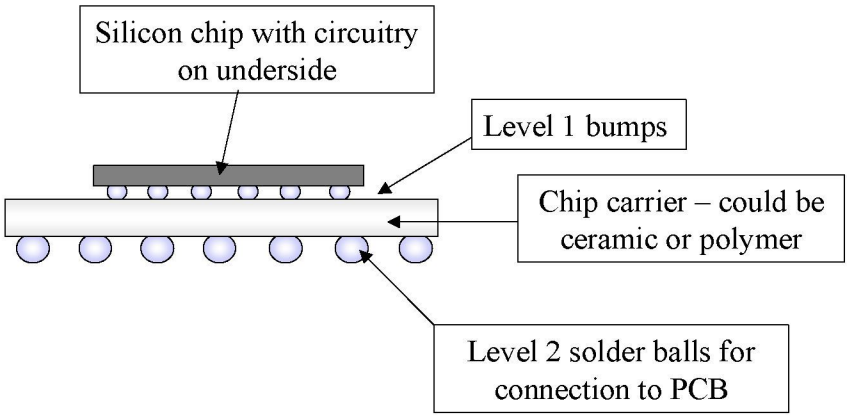

Figure 14. Schematic diagram of interconnection levels from silicon chip to PCB

The Level 2 connections are outside the device and manufacturers are working to convert these to lead-free solder. These joints are generally much larger than those at Level 1. The term flip chip covers a wide range of components and this variation is summarised in Table 4.

Table 4. Characteristics of flip-chip packages

Characteristic	Variety
Silicon chip	Varies in size from less than 2 mm up to 20 mm along one side. Circuitry built up on surface with various materials and complexity. Most advanced flip chip use copper circuitry and many layers.
Bumps	97%Pb3Sn, 90%Pb10%Sn, 63%Sn37%Pb, SnAg, Sn3.5%Ag0.7%Cu (SAC), gold, copper are all used
Attachment of bumps to carrier	Method depends on bump material and substrate. 63Sn37Pb currently used for 97%Pb3%Sn bumps High Pb content solder can be soldered to ceramic at 350°C but low melting point solder is needed for polymer carriers. 63%Sn37%Pb, SnAg and SAC can be soldered directly onto ceramic and organic Gold and copper bumps can be attached using thermocompression bonding or with anisotropically conducting adhesive.
Chip carrier	Ceramic or polymer. There are various types of both of these materials which have different characteristics and so are suitable for different applications.
Level 2 connections	63%Sn37%Pb, SnAgBi, Sn3.5%Ag0.7%Cu (SAC)
Underfill	The gap between the chip and the carrier may be filled by underfill materials. These are adhesives which prevent damage to the bumps and the chip that would otherwise result from the strain imposed by thermal cycling. These need to be compatible with choice of soldering flux (new fluxes are used for lead-free) and adhere to the surface layers on the chip after soldering

Flip-chips range from very small ICs with a small number of bumps and Level 2 interconnections to devices with a large silicon chip and thousands of Level 1 bumps. The technical challenges to change to lead-free flip chip are much greater for the larger more complex flip chip than the small and simple components. Some lead-free flip chip devices are already available commercially from several manufacturers. Most of these are relatively small with few bumps and are used in low power applications where thermal cycling is minimal.

2.9.1 Level 1 connections

The Level 1 connections need:

- High fatigue resistance to survive large numbers of thermal cycles, where there is significant difference in coefficient of thermal expansion between the chip and the chip carrier. Lead is known to provide this fatigue resistance.
- Electromigration resistance[16]. Electromigration is the (slow) movement of the elements of an electrical conductor under the action of an electrical current. The effect becomes more serious as the dimensions of the parts shrink.

- Known long term reliability.

Thermal Fatigue

The coefficient of thermal expansion (TCE) of silicon is very low in comparison with the polymers used for carriers and the PCB. The TCE of ceramic carriers is intermediate between that of silicon and most polymers:

Table 5. Comparison of the thermal coefficient of expansion of package materials

Material	TCE ppm/°C
Silicon	~ 2.5
Ceramics	~ 7
Polymer carriers and PCBs	~ 14

As a result of the differences in TCE, when the temperature changes, a strain is imposed on the bumps, the silicon and the circuitry on the chip surface.

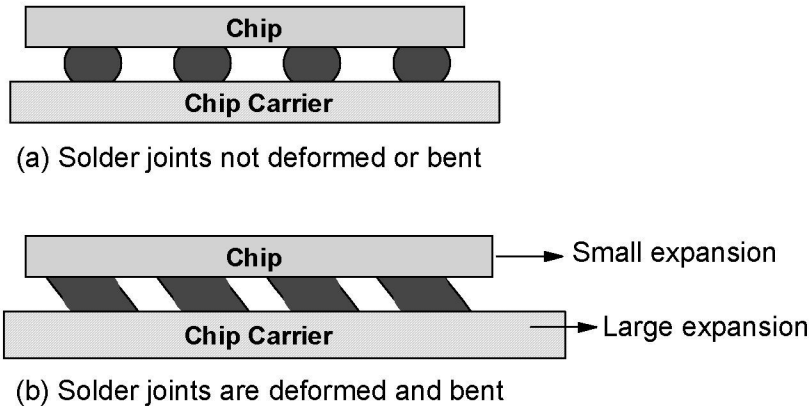

Figure 15. Schematic diagram of interconnection levels from silicon chip to PCB

This strain can cause damage to the silicon (cracks), damage to chip circuitry (particularly the fragile dielectric layers) or cracks within brittle intermetallic layers which tend to be thicker, and so more prone to damage, in lead-free bonds than in tin/lead bonds.

Thermal cycling occurs with most electrical equipment and this can result in thermal fatigue of solders. The thermal fatigue behaviour of lead solders is well understood as these have been used for decades and so both accelerated tests data and field data are available. No field data is available for lead-free solders. High lead content solders are frequently used for the larger size silicon chips because of its superior thermal fatigue life, which is approximately double to three times that of eutectic tin/lead. The difficulties with prediction of field life of lead-free solders from accelerated tests data is discussed in section 2.2.3. Larger silicon flip-chips attached to polymer carriers present a high strain situation and so test data obtained with lead-free solders would indicate that performance would be inferior to eutectic tin/lead and high lead content alloys. In the course of this investigation,

several flip-chip manufacturers provided data which they had obtained with flip chip packages using accelerated testing. In general, smaller die with tin/silver/copper bumps passed test criteria but the field life is of course unknown. However, tests with the largest die caused cracking after very short test periods and this alloy could not be used. In one case, a manufacturer may be forced to change from a solder with 37% lead to a high lead content solder (already exempt from RoHS).

Electromigration

Flip chips with relatively high power requirements use high lead solder bumps because eutectic tin/lead cannot be used due to degradation by electromigration. Electromigration can occur to the thin conducting tracks on silicon chips as well as to the very small solder bumps on flip-chip and is a failure process in which the flow of electrons through the conductor causes the movement of atoms. Different metals move differently and their movement is affected by temperature. At temperatures below 100°C, tin/lead can be separated into tin at one end of the bump and lead at the other but at above 100°C, tin moves in the opposite direction. This makes acceleration of this process very difficult. The movement of atoms eventually leads to the formation of voids or gaps which, under strain, cause cracking and eventually bond failure. As voids form and the bump contact area decreases, the current conduction path is constricted which increases the current density. This can increase the rate of electromigration and also increases the temperature.

Research into electromigration is on-going but results are frequently contradictory. The main obstacle is that it is very difficult to accelerate this process as the main method, increasing temperature, changes the basic electromigration behaviour of metals. High lead content solders are known to be superior to eutectic tin/lead, in one series of tests, by a factor of 100 times (see Figure 16, from Freescale Semiconductors).

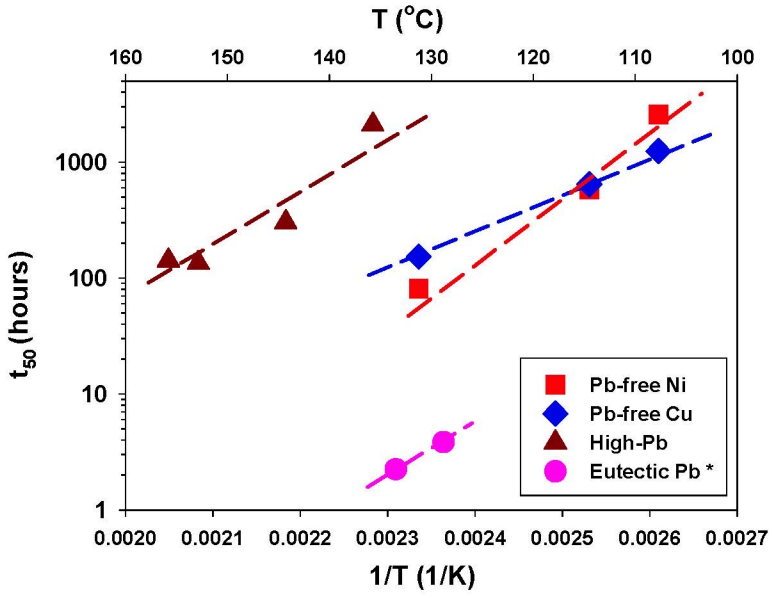

Figure 16. Accelerated electromigration test results (Freescale Semiconductors). Predicted reliability for three alloy types Pb-free is SAC on either copper or nickel

Results obtained with lead-free solders are often contradictory but it appears to be inferior to high lead content solders although it may be superior to eutectic tin/lead but, again, this is not yet certain. Lead-free solders such as tin/silver/copper contain intermetallic crystals which are poor electrical conductors. As a result, the flow of electrons is diverted around these particles which could in theory cause voids to form where current crowding occurs, severely shortening the bond's life.

Research into high lead solder bumps attached to carriers with lead-free solders has not been carried out yet. This would add silver and or copper to the high lead alloy which theoretically would increase electromigration due to intermetallic crystals.

Intermetallics

Eutectic tin lead and high lead content solder such as 97%Pb3%Sn do not contain intermetallic crystals and as a result are ductile materials. The most commonly used lead-free solders contain silver and copper but both form intermetallic crystals and as a result, these alloys are harder and less ductile. Intermetallic crystals are relatively small in comparison with the size of solder joints made between components and PCBs. However, solder flip-chip bumps are typically 60µm diameter and intermetallic crystals can grow to become a significant proportion of these bumps. Ag3Sn intermetallic crystals are needle shaped and so are relatively long (see Figure 17). The length of intermetallic crystals will depend on the temperature and flip chips that operate at higher temperatures may grow relatively large intermetallic crystals. As these crystals are hard and in many cases brittle, if they become relatively thick or occupy a significant volume of the bump, then these may cause cracking and failure if a high strain is applied such as that due to thermal cycling. Manufacturers are currently investigating this to determine what are the limitations that intermetallics will impose. Research should be able to define conditions where intermetallics are not a serious problem and those where they are likely to cause premature failure and hence using these solder alloys would be inappropriate.

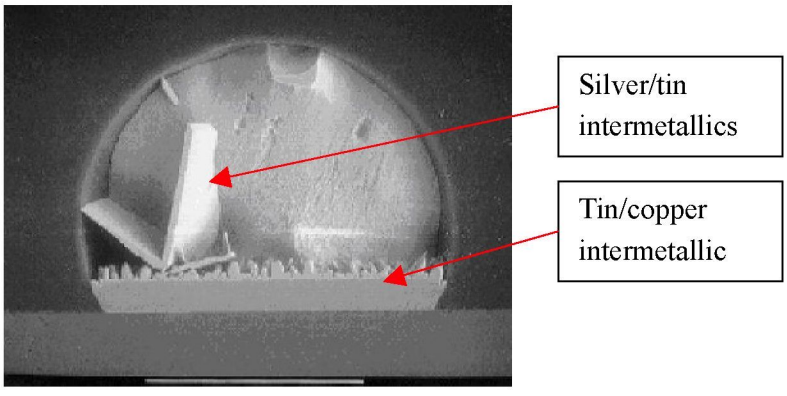

Figure 17. Etched cross-section through SAC bump showing large Ag3Sn intermetallic crystals (from Texas Instruments)

Another concern with very small solder bumps is the formation of voids at the intermetallic / solder interface due to "Kirkendall voids". This effect is known with tin/lead solder but recent studies have

shown that this is worse with lead-free solders. However this defect is apparently intermittent and although could be viewed as another reason to exempt lead in solders, this was not highlighted as a serious concern by any of the flip-chip manufacturers who were consulted.

Damage to Dielectrics

There is an on-going trend with the most advanced flip-chips to use dielectric layers with lower dielectric constant (K). These layers are the insulators between conductor tracks and pads and as the clock speeds of these chips increase, the K values need to be reduced. Air has a very low K and so the low K dielectrics are produced with minute air bubbles as "foam". These materials are relatively fragile, however, and cannot withstand a high strain. Lead-free solders, gold and copper bumps are all harder than eutectic tin/lead and high lead content solders and so will transfer more strain to these layers during assembly and thermal cycling. Damage is seen as cracks or as delamination and both result in failure of the flip-chip.

2.9.2 Alternative bumps

1. Some flip chip packages currently use high melting point solder bumps which are attached directly to ceramic carriers by melting these at 350°C. These alloys are exempt and so this approach can continue. However this is possible only with certain types of flip-chip and ceramic carriers and cannot be used with all types of ceramic. The choice of carrier is complex and depends on many variables but in particular depends on the function of the device.

2. High melting point bumps cannot be attached directly to polymer carriers as the high temperature required to melt the solder would destroy the carrier and therefore a low melting point solder is used. 63%Sn37%Pb solder is used by many of the flip chip manufacturers as reliable bonds can be produced. Figure 16 shows a cross-section through a bond made in this way (from IBM).

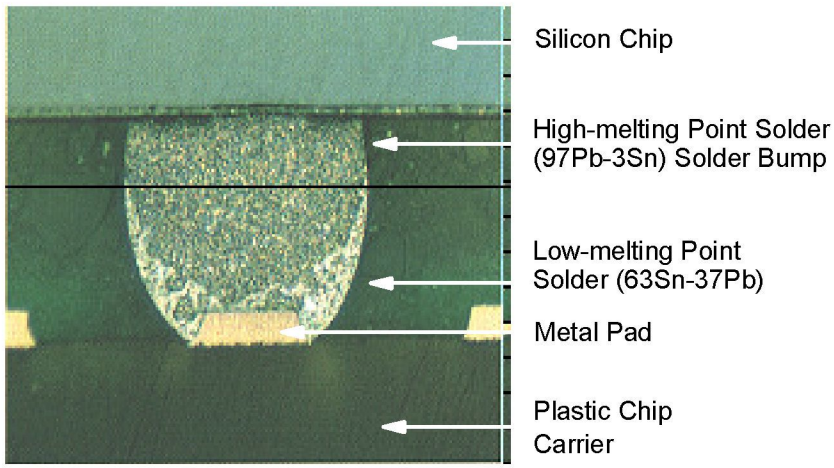

Figure 18. Cross-section through solder bump

The use of 63Sn37Pb solder is not permitted by the RoHS Directive and so, without an exemption, an alternative alloy would be required. Also, the lead content of each bump after bonding the high lead content solder with eutectic solder would contain <85% lead and so may be considered not to be covered by the existing exemption included in the RoHS Directive Annex.

Manufacturers have considered the use of, for example tin/silver/copper lead-free solders to attach the high melting point solder bumps to carriers as an alternative approach. However, this would produce a combination of elements that is new, with no research data available. Also, there is no field data on the long term reliability of these bonds. Without this data, there is a potential risk to consumer safety when these components are used in safety critical equipment. The addition of silver would produce intermetallics as well as hardening the material, both of which could potentially reduce reliability.

3. Several manufacturers currently use 63Sn37Pb bumps but have been evaluating tin/silver/copper (SAC) bumps as an alternative material. One flip chip manufacturer uses tin/silver bumps. Both of these alloy bumps are used in commercially available flip chip packages but the thermal fatigue reliability is not known for the reasons discussed in this report and may be poor, particularly for larger more complex devices.

   Chip size is an important variable. Unpublished research data which was provided by two manufacturers showed that, in accelerated thermal fatigue tests, silicon die of 11 – 15 mm along each side bonded with SAC bumps did not fail the test whereas silicon die of side 20 mm rapidly failed due to thermal fatigue.

4. Gold bumps are used by a few flip chip manufacturers but all of these devices have relatively small numbers of bumps. Gold bumps are produced using the same technique as is used to attach wire bonds to ICs and is a very reliable process. Attachment of a gold bumped chip to the carrier is relatively new technology and, although it is possible where there are a few bumps only, this may not be straightforward where the number of bumps is large as the technique used to create the bond applies force and ultrasonic energy which has the potential to damage the fragile dielectrics on the chip surface, particularly with the more complex devices which have many layers. Also, long term reliability is unknown for this relatively new approach.

   There is a significant cost disadvantage. Solder bumps can be applied to each silicon wafer simultaneously, one wafer may produce 1000 die each with typically 5000 bumps and therefore 5,000,000 bumps can be produced within a relatively short period of time whereas each gold bump is attached one at a time and it is estimated that application of gold bumps to a wafer would take at least 20 times longer and so would require 20 production lines instead of 1 for the same productivity. This would require a very considerable investment. The cost of gold is also a consideration but on simple flip chip is not very significant. Research has been carried with copper bumps and flip chip using relatively small numbers of copper bumps have been successfully produced on a laboratory scale. Much more work is required however to develop a reliable manufacturing process. This is analogous to the use of copper for wire bonds which,

although it can be achieved on a small scale, is not widely used as production yields are lower and fine copper wire is susceptible to corrosion.

2.9.3 Level 2 connections

Some semiconductor packages use high melting point solder spheres or columns to make electrical connections to the printed circuit board (PCB). The advantages of this type of connection are:

- Many more connections can be make to one package than if connections are made only at the periphery.
- High melting point solder is ductile and has a very good resistance to thermal fatigue damage. Repeated temperature changes result in stress/strain cycles because of the thermal coefficient of expansion differences between package and substrate which causes thermal fatigue.
- When the package is soldered to the PCB using a standard solder, which could be a lead-free solder, the high melting point solder does not melt maintaining the gap between the package and PCB. This is an advantage because sideways movements due to temperature changes and TCE mismatch will cause less strain with a large gap between PCB and package.

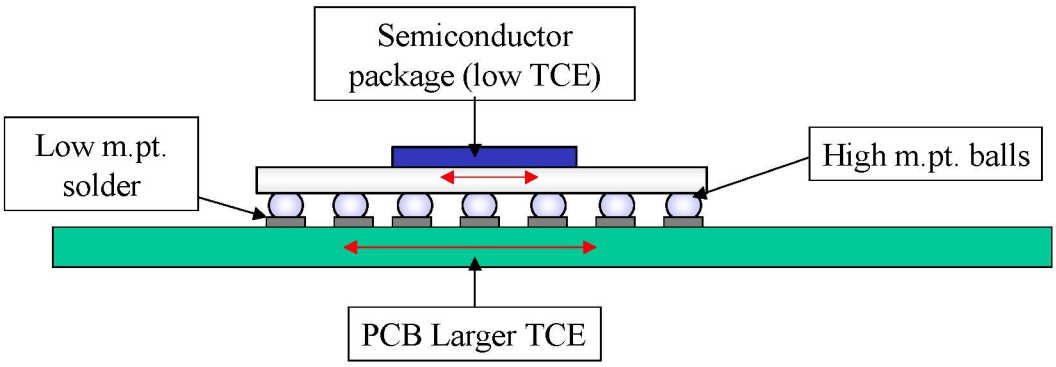

Figure 19. Attachment of Level 2 high melting temperature solder balls to PCB with a low melting temperature solder

In this application, the high melting point solder balls or columns (such as 95%Pb5%Sn) contain >85% lead and so are exempt from the RoHS Directive. A lead-free solder such as Sn3.5%Ag0.7%Cu could be used as the low melting temperature solder which would also be acceptable for the RoHS Directive. However, when the low melting point solder melts, there will be some local melting of the solder ball or column at the interface and some mixing and diffusion of metals so that the metal composition in the vicinity of the interface will contain <85% lead.

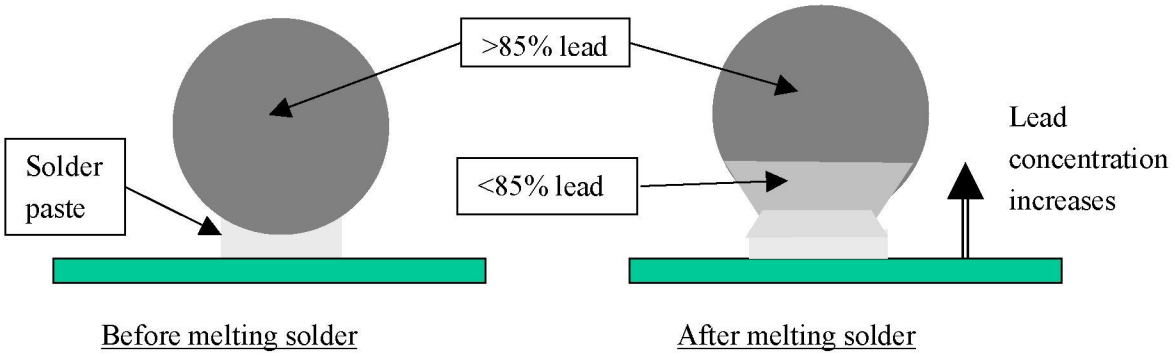

Figure 20. Composition of Level 2 solder ball before and after assembly

In this process, two materials – high lead content solder and lead-free solder have been used, both of which are compatible the RoHS Directive. However, if the alloy composition were to be analysed during market surveillance, the solder bond would be found to contain lead at a concentration of approximately 60 – 70%. The enforcement authority may conclude from this result that the equipment does not comply with the RoHS Directive but it is unclear whether this requires an exemption as two acceptable materials are used.

2.9.4 Alternatives for level 2 connections

One alternative connection technology for semiconductor packages having large numbers of electrical connections would be to use lead-free solder instead of the exempt high melting point solder. These would fully melt during the reflow which could significantly reduce the distance between the chip carrier and the PCB and as explained above, this could be affect long term reliability.

All flip-chip manufacturers who were consulted during this study were asked what their plans were for level 2 connections. Most of the flip-chip manufacturers have developed lead-free level 2 connection technology, although there are a small number of package types where high melting temperature solder cannot yet be replaced. Alternatives include tin/silver/copper balls and, although these melt during reflow, the stand-off height can be achieved in some cases by modification of ball and pad dimensions. IBM has developed an alternative to lead alloy column arrays which are replaced by copper columns[17].

Packages with electrical connections at the periphery are the other alternative as these "lead-frame" (NB "lead" does not mean Pb in this context) components are connected to the PCB with lead-free solders. However, to achieve the same number of electrical connections, the package size would need to be increased significantly, even with a very fine pitch, which may be susceptible to tin whiskers (see section 2.2.3). A larger component size would occupy a larger area of the PCB; this may not be possible in compact equipment and require the use of more materials and generate more waste, some hazardous, during production and at end of life.

2.9.5 Summary of the case for an exemption

Two exemptions have been requested for flip chip packages. One, with no proposed expiry date is for higher power flip-chips that need to use high lead content solder bumps to prevent electromigration in combination with eutectic tin/lead solder. The second exemption request is for lower power flip chip connections which currently use eutectic tin/lead bumps and the original exemption application has a suggested expiry date of 2010.

Higher power flip chip – currently there is no lead-free alternative and lead based alloys may be the only viable option as no other known materials meet all of the essential requirements.

Lower power flip chip – tin/silver/copper and tin/silver may be suitable in some applications but there is no long term field data available and it is not yet known whether accelerated test results can be extrapolated reliably. One manufacturer who produces the largest flip chip die on the market has evaluated tin/silver/copper and tin/silver bumps but, due to the high stress that results from the very large die size, both solder alloys are unsuitable as cracks rapidly form within these lead-free bumps and it appears that a lead-free alternative may not be found for all types of lower power flip-chip package currently on the market.

The wording of the first exemption would also covers level 2 connections of flip-chip and other package types. Manufacturers use high lead solder balls and columns to attach various types of devices to PCBs (Level 2 connections). Most have found that they are able to reliably replace lead solders with lead-free solders and a few have been selling these components for over a year. Clearly a lead-free alternative is possible for most, and probably all level 2 connections.

If a high melting temperature solder ball were to be soldered to the PCB using a lead-free solder such as tin/silver/copper and a reliable joint produced (as found by at least one BGA manufacturer), two acceptable materials would have been used to produce the solder joints and although there will be material with <85% lead and >0.1% lead at the interface, it is unclear whether a separate exemption is needed for this.

2.9.6 Possible alternative wording for proposed new exemptions 10 and 11 (from list in section 1)

The wording used for these two exemption requests would be satisfactory but their interpretation is unclear and could be misleading. Therefore an alternative is suggested for level 1 flip chip connections:

> Flip chip Level 1 connections only
>
> **"Lead in solders to complete a viable electrical connection between semiconductor die and carrier within integrated circuit Flip Chip packages"**
>
> It is possible that no substitute for lead can be found and so no exemption expiry date is suggested although the Commission should review all exemptions at least every four years.

Level 2 connections for Flip chip and certain other package types may not require an exemption as most of the manufacturers consulted have already developed lead-free alternatives. Possible wording to cover the connections between high melting temperature solders and lead free solders could be:

> **"Lead in component external connections made from high melting point solder containing >85% lead and a lead-free solder containing <0.1% lead"**
>
> This reworded exemption is for situations where a manufacturer combines an exempt high melting point solder with a lead-free solder which will create a bond which may have <85% lead, however most flip-chip manufacturers expect to have replaced high melting point solder balls (ball grid arrays) with lead-free alternatives before the 1st July 2006.

connections to PCBs without soldering but which can be removed and re-inserted without damage to the connector or the PCB.

4.5 Lead as a coating material for the thermal conduction module C-ring

Thermal conduction modules are the central processor units used in the Z-Series main-frame computers produced by IBM. The C-ring is the seal used between the glass-ceramic circuit and the liquid cooled copper plate, which is used to remove heat from the semiconductor chips.

4.6 Lead and cadmium in optical and filter glass

Optical components used in electrical equipment such as glass lenses, optical filters and prisms where no lead-free alternative is suitable. Lead in the glass of electronic components is not included in this exemption as this is covered by item 5 of the Annex of the RoHS Directive.

4.7 Optical transceivers for industrial applications

This exemption request was made to cover optical transceivers and the solder connections made to the PCB to which they are attached. Optical transceivers convert optical signals into electrical signals using glass-fibre connected to a photosensitive semiconductor, convert electrical signals into optical signals using a laser diode or LED attached to an optical fibre or one device may contain both functions.

4.8 Lead in solders consisting of more than two elements for the connection between the pins and the package of microprocessors with a lead content of more than 85% in the proportion to the tin-lead content (exemption until 2010)

A lead-based solder with a melting point higher than standard lead-free solders and eutectic tin/lead but containing <85% lead which is used to attach pins to the carriers of microprocessor packages. This alloy is not covered by the exemption listed as item 7.1 of the Annex of the RoHS Directive which is for solders which contain >85% lead (see section 1.3).

4.9 Lead in high melting temperature type solders (i.e. tin-lead solder alloys containing more than 85% lead) and any lower melting temperature solder required to be used with high melting temperature solder to complete a viable electrical connection

This exemption is intended for internal (Level 1) connections made between the semiconductor die and the carrier in flip-chip packages which have higher power consumption and currently use high melting temperature solder bumps (>85% lead) which are connected to the carrier with eutectic tin/lead (~37% lead). The bump composition will have <85% lead. This exemption would also include situations where high melting point solder balls (e.g. on ball grid array packages) are attached to a PCB with a lead-free solder. It is not intended to permit the use of solders containing lead for

making electrical connections to PCBs unless the low melting point solder is attached directly to the high melting temperature solder. Although the description states "all low melting temperature solders", this is not intended to include cadmium based solders.

4.10 Lead in solders to complete a viable electrical connection internal to certain integrated circuit packages (Flip Chips)

For internal (Level 1) connections made between semiconductor die to carrier in flip-chip packages which have lower power consumption and currently use eutectic tin/lead solder bumps. Currently eutectic tin/lead solder (37% lead) bumps are used.

4.11 Proposed alternative flip-chip exemption titles

As the previous two proposed exemptions are intended primarily for Level 1 connections in flip chip packages and information received during this study has shown the first of these is being misinterpreted, two alternative descriptions have been suggested:

- **Lead in solders to complete a viable electrical connection between semiconductor die and carrier within integrated circuit Flip Chip packages**

  This refers to lead in solder used for internal Level 1 interconnections within most types of flip-chip packages.

- **Lead in component external connections made from high melting point solder containing >85% lead and a lead-free solder containing <0.1% lead**

  Where an external connection to a component (flip-chip and others) uses a high melting point solder containing >85% lead is connected to a PCB using a lead-free solder. This combination of materials produces a solder composition at the interface containing <85% lead. This is used to maintain the stand-off height of components to reduce the risk of damage by thermal fatigue from thermal cycling but most component manufacturers who have been consulted have stated they have developed lead-free alternatives and so this exemption may not be required.

4.12 Safety equipment for fire and rescue services

Equipment used by fire and rescue services, in the field, that would otherwise be within the scope of the RoHS Directive. This would include telecommunications and GPS equipment.